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X-Ray Upgrade Can See Transistors in 3D › You can now make a map of even the most advanced chips without destroying them

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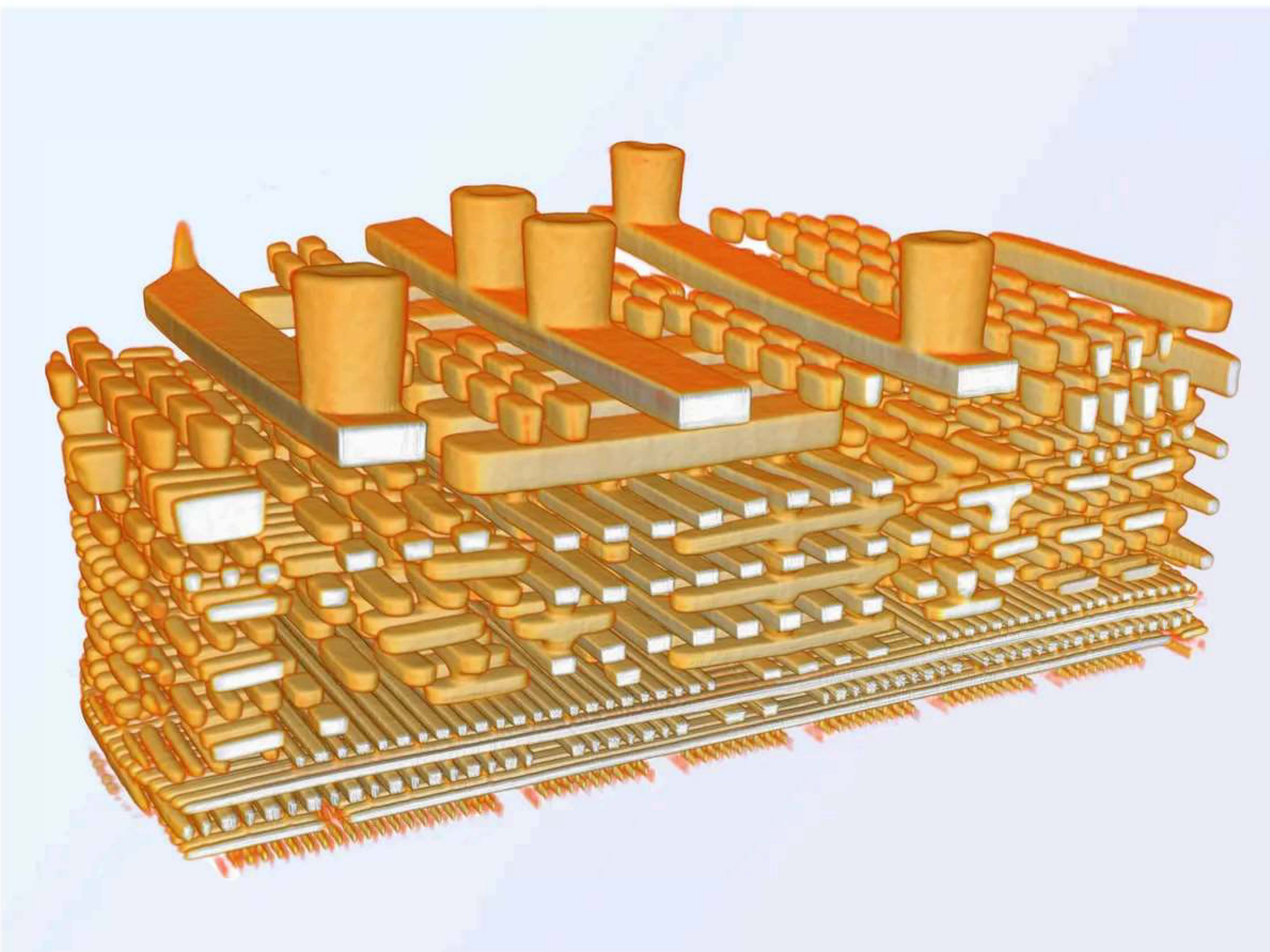

A 4-nanometer resolution X-ray technique can render a chip's inner workings from the large interconnects at the top to the transistors at the bottom.
PAUL SCHERRER INSTITUTE

AN UPGRADED X-RAY IMAGING TECHNIQUE CAN provide crisp, 3D images of the inner workings of chips, revealing their designs and their flaws. The method has a resolution of 4 nanometers, providing images clear enough to map a chip's wiring paths and reveal tiny transistor features without destroying the chip.

A team of scientists at Paul Scherrer Institute, including Tomas Aidukas and Mirko Holler, developed the improved imaging technique along with University of Southern California's Tony Levi and ETH Zürich's Gabriel Aeppli. It builds on an earlier method developed by largely the same team, called ptychographic X-ray laminography (PyXL). Levi says they wanted to provide an alternative to the time consuming, destructive processes used to perform quality control and reveal chip designs.

Using the state of the art chip imaging techniques, "you really need to know what you're looking for ahead of time," says Baohua Niu, a principle engineer at the Intel Foundry, in Hillsboro, Ore., who was not involved with the research.

Today's chips are so complicated that electrical tests alone can't pinpoint where a defect is, he says. Engineers use a mix of optical imaging and other methods to zero in on potential problem areas. They then image that part of a chip's surface with scanning electron microscopy, and finally take a slice of a chip for further imaging with a transmission electron microscope (TEM). When they find the flaw, they can then go back and correct their design.

The new imaging technique uses "hard" or high energy X-rays produced at a particle accelerator called a synchrotron. These beams can penetrate all the way through a chip, no slicing required. "Unlike with an optical microscope, it's very difficult to make lenses," Levi says of the X-ray range. His group's method works by repeatedly illuminating the sample from different angles with a coherent beam of high energy X-rays. Tiny features in the chip diffract the light. Algorithms then reconstruct the most likely version of the image based on the intensity and phase of the diffracted X-rays. This kind of imaging is generally called ptychography.

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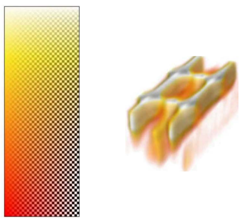
-TONY LEVI, UNIVERSITY OF SOUTHERN CALIFORNIA

The initial version of this imaging technique, PyXL, provided a resolution of about 19 nm, says Levi—good enough to discern a chip's interconnects but too coarse to zero in on individual transistors' features. To drive the resolution down further, the team sought to remove a major source of noise, tiny vibrations that can blur the image.

The solution they found, called burst ptychography, was to take images in bursts, and then use computational methods to sort them out. "We take multiple short duration pictures, stack them together, and remove the jitter to get a stable diffraction pattern," says Levi. This enabled the resolution of 4 nm they reported this week in *Nature*; Levi believes the team has a path to get to 1 nm resolution.

Intel's Niu says the resolution of this ptychographic X-ray computed tomography technique is 4 or 5 times lower than that provided by a TEM. But that trade-off is worth it because the technique doesn't require cutting up and destroying the chip, and can provide much deeper 3D images: Engineers can see through the entire 5 micrometer depth of chip, as opposed to the 10 to 30 nm depth visible under a TEM.



Burst ptychography reveals the transistor fins and gate contacts[right]. The color[left bar] is electron density in charges per cubic angstrom. PAUL SCHERRER INSTITUTE

Niu's team at Intel implements new processes and works to improve chip yield and performance. He says the new method should make it easier and faster for engineers to find chip flaws. Manufacturing processes don't always result in the features designers were aiming for, and imaging can help engineers bring designs and reality closer together. "Here's what you designed for; here's what actually was made given your design," he says. "It gives you physical validation."

The team used the method to image an AMD Ryzen 5 processor made using TSMC's 7-nanometer node process. The results included details of the structure and features of its FinFET transistors. These images can be quite revealing, says Levi. “You can see how precisely they placed the metal. With this resolution you can see how well the transistors are put together and what materials they are using.” The X-ray images can also reveal the web of interconnects, metal wires that connect transistors on a chip. “The way things are connected tells you how the chip works,” he says.

“You can figure out how good the engineering is, and the manufacturing. You can see the quality in one chip, the slipshod in another,” say Levi.

Getting a 3D view at higher resolution is becoming more important as transistors and chips gain more 3D features, says Niu. Transistors keep getting smaller and are no longer planar —both FinFETs and upcoming gate all-around transistors jut up from the surface or are layered. And semiconductor manufacturers including Intel are planning on moving chips’ power supplying interconnects from the front to the back side of chips in coming generations, adding an additional layer of complexity.

“Metrology is key to continue progress in semiconductor manufacturing,” says Niu. Burst ptychography “is a very good research effort to meet a critical need. What you cannot measure you cannot improve.“