Toward Long-Term Retention-Time Single-Electron-Memory Devices Based on Nitrided Nanocrystalline Silicon Dots

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***Abstract*—A memory capacitor with a structure of Si–SiO_2/nc-Si dots/silicon nitride films/SiO_2 was prepared by means of nc-Si dot deposition followed by N_2 plasma nitridation processes. The memory device offers dual memory nodes: nc-Si dots and traps in silicon–nitride films. An enlarged memory window in *CV* characteristics was observed in memory operations, due to the extra traps in silicon–nitrides. The charge-loss rate was found to be much smaller than that of single memory nodes using nc-Si dots only. The provided larger memory window (about twice the width) and longer retention time in the memory operations (three orders of magnitude) are discussed in terms of trap-assisted charging/discharging mechanisms.**

***Index Terms*—Charge carrier processes, memories, MOS devices, nanotechnology, quantum dots.**

I. Introduction

BOTH nanocrystalline silicon (nc-Si) dot [1] and oxide-silicon nitride-tunnel oxide (ONO) [2] based nonvolatile memory devices have received much attention recently as a result of continued scaling of MOSFETs where nc-Si dots and traps of nitrides, respectively, act as discrete memory nodes. In these kinds of devices, stored electrons can be operated one by one, and few or even one single electron can guarantee a reliable memory state, referred to as the single electron memory (SEM) [3], [4]. However, in spite of the successful demonstrations of memory operations and obvious advantages, the charge retention time of both memories is too short for practical nonvolatile memory applications [1]–[4]. To improve charge retention time with little cost of the write/erase time, it is possible to take advantage of trap-assisted charging/discharging operations [5] that need thermal excitation processes. Nevertheless, the ONO based memories suffer from a higher operation voltage, due to the larger dielectric constants for Si_3N_4 ($\varepsilon_{\rm nd} = 7.5$) than for SiO_2 ($\varepsilon_{\rm ox} = 3.9$), and unknown trap distributions, which always give rise to variations in the threshold voltage between devices. nc-Si dot based memories can offer a well-controlled memory node positioning, relying on modern nanotechnologies [6], [7]. Therefore, a memory architecture using nc-Si dots covered by silicon–nitride films (dual memory nodes) as a floating gate may provide improved memory operations, where interfacial traps are intentionally introduced in terms of ultrathin nitride by N_2 plasma nitridations on the nc-Si dots during device fabrication. The nitride system is commonly known to have a higher density of localized defect sites, but discharge properties are roughly similar to the Si–SiO_2 system [8]. Therefore, a nominal number of trap sites from ultrathin nitride on the dots may contribute in charge retention, but not degrade the device reliability or performance considerably [9]. Detailed investigation is encouraged to understand clearly the charge retention behavior and the transport mechanisms between the trap and the dot and between the dot and the channel.

Manuscript received June 5, 2003; revised November 19, 2003. This work was supported in part by a grant-in-aid for Scientific Research from the Ministry of Education and in part by the Core Research for Evolutional Science and Technology (CREST) program of the Japan Science and Technology Corporation (JST).

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Digital Object Identifier 10.1109/TNANO.2004.824037

II. Experimental Details

A memory device with a SiO_2/silicon nitrides/nc-Si dots/SiO_2 structure on a silicon substrate has been chosen for these studies. This structure potentially serves as the floating gate in nonvolatile SEM devices [10]. Fig. 1(a) shows the schematic of the device structure comprised of nc-Si dots and silicon–nitrides. The device fabrication process began with a $\langle 100 \rangle$ p-type silicon wafer with an acceptor concentration of 1.5×10^{15} $\rm cm^{-3}$. After using H_2SO_4/H_2O_2 (30:70) and diluted HF solution cleaning processes, an ultrathin tunnel oxide of thickness $\sim$2 nm was grown by H_2SO_4/H_2O_2 (30:70) oxidization for 10 min at 130 °C. Next, a layer of nc-Si dots was deposited by very high-frequency plasma decomposition of silane (SiH_4) [11]. The nc-Si dots just after depositions were 8 nm in diameter with a narrow size distribution and a density of $1.1 \times 10^{11}/\rm cm^2$ as observed by scanning electron microscope [Fig. 1(b)]. The surface portion covered by nc-Si dots was estimated to be 7%. Subsequently, the sample was placed into nitrogen plasma ambient (r.f. = 13.56 MHz, Power = 2.6 W/$\rm cm^3$) for 20 min at substrate temperature of 800 °C, which gave rise to 1-nm silicon–nitride films on the nc-Si dots. For comparisons, control samples without nc-Si dots or nitridations were also fabricated following the same processes. Then a 45-nm-thick upper-oxide was deposited by plasma enhanced CVD using TEOS as gas source, and the samples were annealed in N_2 ambient at 1100 °C for 1 h, to improve the quality of thus-prepared SiO_2. Aluminum electrodes for the front (gate electrodes, 100 μm in diameter) and the back sides were deposited after etching away the SiO_2 on the wafer backside, which also reduced the upper-oxide thickness to 41 nm. Finally, samples were annealed again in a

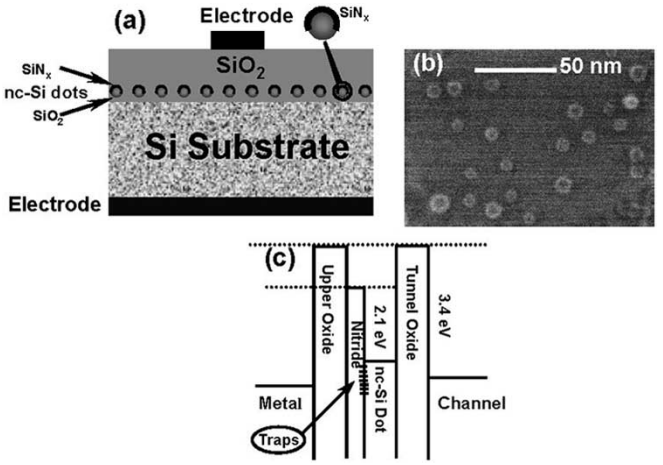

Fig. 1. (a) Schematic of Si–SiO_2/nc-Si dots/silicon–nitride/SiO_2 sample structure. nc-Si dots were covered by silicon–nitrides. (b) A scanning electron microscopy image of the nc-Si dots. (c) Schematic of the band diagram, in which the band bending are not taken into account.

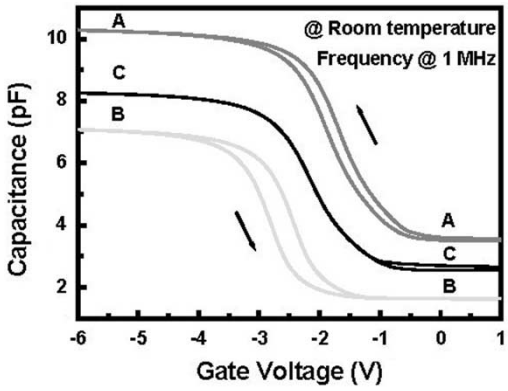

Fig. 2. *CV* characteristics of three samples measured at same scan range and speed. The vertical shift of *CV* curves is due to the effective thickness difference of the SiO_2/nc-Si dots (silicon–nitride)/SiO_2 structures. Here, samples are denoted by A (nc-Si dot deposition without nitridation), B (nc-Si dot deposition followed by nitridation), and C (nitridation without nc-Si dot deposition).

H_2/N_2 ambient at 450 °C for 5 min, which improved the contact properties of the devices. In this paper, three samples were prepared, denoted by A (nc-Si dot deposition without nitridation), B (nc-Si dot deposition followed by nitridation), and C (nitridation without nc-Si dot deposition). The electrical properties of the memory devices were measured with an HP4156B precision semiconductor parameter analyzer and an HP4284A precision LCR meter at room temperature.

III. Results and Discussions

The results of Si2p X-ray photoelectron spectroscopy (XPS) spectrum analysis identified that the Si–N bond presented in nitrided nc-Si dots. Moreover, silicon–nitride films prepared on a naked silicon surface under identical conditions were nearly stoichiometric. These will be discussed elsewhere in the details [12]. Since the bottom of nc-Si dots contacted with the tunnel oxide layer and the other parts were nitrided by nitrogen plasma, the introduced nitride traps were only distributed on the top or sides of nc-Si dots, as shown in Fig. 1(c). Taking the ultrathin thickness of silicon–nitrides and the defect density of about 10^{11}–10^{12} cm^{-2} into account [13], there were roughly one or two defects located on each of nc-Si dots.

High-frequency capacitance-voltage (*CV*) measurements were performed at room temperature to investigate memory operations as shown in Fig. 2. The density of positive fix charges (Q_f) in the device can be calculated according to the sample C (with nitridation, without nc-Si dots) as follows [14]:

$$Q_f = \frac{(V_{\rm FB} + 2V_B - V_T) \times C_{\rm ox}}{e} \tag{1}$$

where, e is the elementary charge (1.6×10^{-19} C), $V_{\rm FB}$ is the flat-band voltage, V_B is the energy separation between the Fermi level and the center of forbidden-band of the substrate, V_T is the take-off voltage of *CV* curves, and $C_{\rm ox}$ is the maximum capacitance per unit. From the experimental results and the acceptor density, $V_{\rm FB} = -1.96$ V, $V_B = -0.3$ V, $V_T = -0.92$ V, and $C_{\rm ox} = 1.052 \times 10^{-7}$ F/cm^2 are calculated. Therefore, the density of the positive fix charge is 7.5×10^{11} cm^{-2}, which is similar with what was reported on the defect density of silicon–nitride films [13].

Before discussing the features of Fig. 2, it is worthwhile to point out that there is a little difference in the maximum capacitance $(C_{\rm max})$ and the minimum capacitance $(C_{\rm min})$ of sample A, B, and C. According to the experimental results of $C_{\rm max}$, the effective SiO_2 thickness was calculated to be 31.8 nm (sample A), 45.9 nm (sample B), and 39.7 nm (sample C), where the extension of electrodes (about 10% in the diameter) in the metal evaporation processes was considered. Therefore, the geometric structure of gate-oxide thickness, of approximately 40 nm of sample C, is consistent with the effective thickness. On the other hand, effective thickness directly correlates with gate leakage. The reduction of the effective thickness of sample A may be attributed to the embedded nc-Si dots that are conductors within the insulator, however remains unclear. Meanwhile, silicon–nitrides on the SiO_2 and Si surface were known as anti-leakage layers. The increase of the effective thickness of sample B could be derived from the shielding silicon–nitrides of sample B. As a consequence, the different $C_{\rm min}$ of each sample may result from the different effective thickness of the dielectric layer due to different embedded layers or parasitic capacitances of embedded layers, however this also still remains unclear.

The observed flat-band voltage is a combined effect of changes in $C_{\rm max}$ and $C_{\rm min}$. However, the shift of the flat-band voltage $(\Delta V_{\rm FB})$, which results from the charge storage in the memory nodes, is not affected by $C_{\rm max}$ or $C_{\rm min}$, since these variable influences in each sample are negligible through subtraction of backward $V_{\rm FB}$ and forward $V_{\rm FB}$. In other words, if we only focus on the storage of charge in the memory nodes, the change of $C_{\rm max}$ between samples mainly from the bottom layers of nc-Si dots and tunneling oxide, is trivial. The charge storage and retention characteristics are comparable in samples A, B, and C.

In Fig. 2, a clear hysteresis in *CV* curves was found at the flat-band voltage shift $(\Delta V_{\rm FB})$ of 0.196 V in sample A, which is consistent with our previous work in which the hysteresis could be attributed to electrons stored in the embedded nc-Si dots [15]. However, contrary to what was expected

in conventional metal-oxide-nitride-oxide-semiconductor (MONOS) memories, where the floating silicon–nitride films offer defects as memory nodes, no flat-band voltage shift was observed under identical measurement conditions in sample C. This may result from a smaller number of defects provided by the ultrathin silicon–nitride film, especially for the direct nitridation on the SiO_2 surface [16]. The hydrogen or oxygen passivation effects in the fabrication processes may be another reason for no hysteresis found in sample C, where the defects from dangling-bands are passivated [17], [18]. It is interesting to point out that the significant increase of the memory window of *CV* characteristics of $\Delta V_{\rm FB} = 0.372$ V can be found in sample B compared to sample A. This implies that traps in surrounding silicon–nitride films can offer extra carrier trap sites and thus enlarge the flat-band voltage shift in the memory operations.

According to a model of fixed charges in the floating gate [1], one can estimate the theoretical magnitude of flat-band shift ($\Delta V_{\rm FB}^{T}$) for one electron per nc-Si dot with the formula

$$\Delta V_{\rm FB}^{T} = \frac{e n_{\rm dot}}{\varepsilon_{\rm up}} \left(t_{\rm upper} + \frac{1}{2} \frac{\varepsilon_{\rm up}}{\varepsilon_{\rm Si}} t_{\rm dot} \right) \tag{2}$$

where $n_{\rm dot}$ is the density of the nc-Si, $t_{\rm upper}$ is the upper gate oxide thickness, $t_{\rm dot}$ is the nc-Si dot diameter, $\varepsilon_{\rm up}$ and $\varepsilon_{\rm Si} = 11.7$ are the permittivities of upper oxide and nc-Si dot, respectively. The nc-Si dot diameters are 8 nm for sample A and 7 nm for sample B. 1 nm reduction of sample B is due to nitridation processes. For sample A, the permittivity of the upper dielectric layer SiO_2 is $\varepsilon_{\rm up} = \varepsilon_{\rm ox}$, In sample B, taking thick upper silicon–dioxide and ultrathin silicon–nitride multilayers into account, the upper dielectric layer's permittivity is also employed to be 3.9 [16]. From this model, $\Delta V_{\rm FB}^{T}$ is calculated for the present density of dots to be 0.242 V for sample A. According to the experimentally measured flat-band shift ($\Delta V_{\rm FB} = 0.196$ V) under maximum positive gate voltage, it suggests that 80% of the nc-Si dots are charged in sample A. On the other hand, the flat-band voltage shift measured in sample $B, \Delta V_{\rm FB} = 0.372$ V, is much greater than what was calculated ($\Delta V_{\rm FB}^{T} = 0.241$ V) based on the trap site density only provided by nc-Si dots. Taking the structure difference between samples A and B into account, it is reasonable to attribute the extra flat-band voltage shift to the provided trap sites from silicon–nitride defects. The additional trap-site density is also consistent with the defect density of silicon–nitride.

While a gradually changing voltage was added on the gate electrode, current–voltage (*I–V*) characteristics of the three samples were measured at room temperature, as shown in Fig. 3. The gate-voltage scan started from -5 to 2 then back to -5 V. Since the investigated sandwiched structure has a very large resistance due to the large oxide thickness ($\sim$ 41 nm), the observed current in these experiments is the displacement current. As shown in Fig. 3(b), neither direction-dependent current nor current peaks were observed in sample C. Therefore, *I–V* and *CV* characteristics of sample C clearly show that the nitrided side tunnel-oxide-films (the area which was not occupied by nc-Si dots) do not manifest any memory effects and as a result

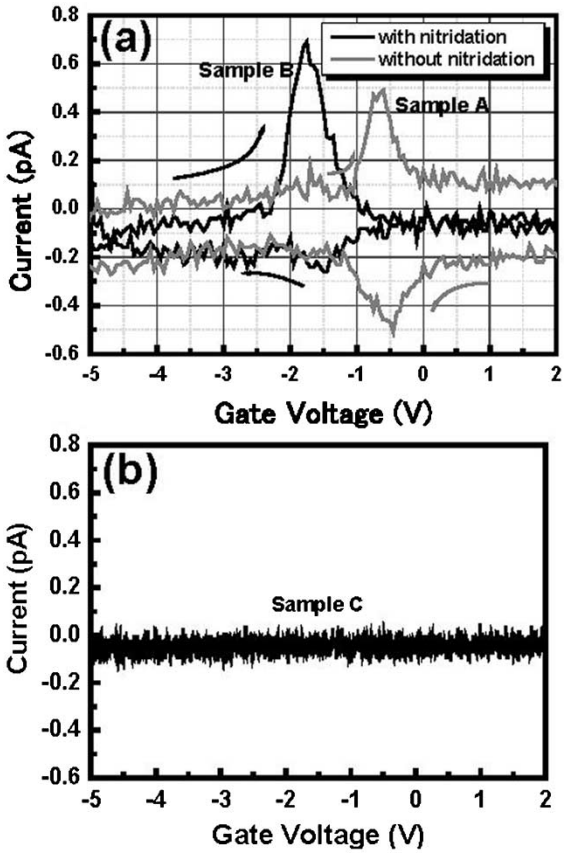

Fig. 3. The room temperature displacement current through samples at voltage step of 50 mV (hold time of 10 ms and delay time of 10 ms). (a) Comparison of samples A and B. (b) Sample C.

do not contribute to charge-retention. In contrast, a pair of current peaks with the same heights was observed in each forward and backward voltage-scans of sample A. The peaks locate at -0.689 V for forward-scan (uncharged state) and -0.460 V for backward-scan (changed state). Thus, the peak-position shift resulting from the stored charges is 0.229 V, which is consistent with what was observed in the flat-band voltage shift of *CV* characteristics and calculated theoretical results. In sample B, however, in spite of an existing similar pair of current peaks, the height of the discharge peak in the backward-scan is smaller than that of the charge peak in the forward-scan [Fig. 3(a)]. These results hint to understanding the enlarged hysteresis windows in *CV* characteristics. According to Gauss' law for the electric field, the displacement current is proportional to the number of movable charges across the vertical structure, which can respond to a varied electric field. The smaller current height indicates that some of the charge remained and localized in the memory nodes of sample B in the erase programs instead of totally being delocalized within the entire nc-Si dot as in sample A. The localized charge in the memory nodes did not respond to the change of the electric field. The other charges trapped in nc-Si dots contribute to the measurable displacement current, which result in a smaller height in the discharge current peak. We suggest that in the write program, after electrons are charged into the nc-Si dots, some stored electrons are polarized to the top of the dot then fall into traps in the same region. The stored electrons in traps of silicon–nitride films would be localized at the

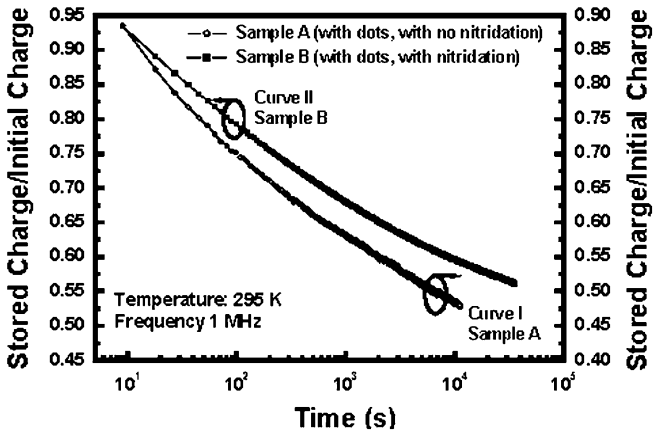

Fig. 4. Time dependences of the stored-charge from the flat-band state, after electrons were injected into floating-gates, shows a logarithmic discharging behavior. The gate voltage was maintained at the initial flat-band voltage: -1.6 V for sample A (solid square symbol) and -2.4 V for sample B (open circle symbol).

defect energy level and face a higher thermionic barrier. Therefore, few are released from the floating memory-nodes, which provide the possibility of long-term retention-time.

To understand the difference in the charging and discharging processes from nc-Si dots and traps of nitrides, a time dependence of stored-charge from the flat-band state, due to the electrons tunneling back to the Si channel, was measured at room temperature. After the memory nodes were filled with electrons at a write-voltage of $+3$ V, the capacitance was measured at the initial flat-band voltage of -1.6 V and -2.4 V for samples A and B, respectively. The measured capacitance was converted to be a ratio of the stored charge to the initial stored-charge, as shown in Fig. 4. The capacitance is represented by a linear function with exponential time elapse. It can be found that curve I, corresponding to the discharging of sample A, presents a steeper slope than curve II, corresponding to sample B, which indicates that the charge-loss rate is larger in sample A. Generally, the retention time was defined as elapsed time when the memory window disappeared [17], [19]. The careful analysis on the Shi and Ohba's results in aforementioned lectures showed that the memory window usually disappeared when at most 40% charge remained in the memory nodes. Considering that the electron injection-rate is usually smaller than the loss-rate, it is also reasonable to suppose that the memory window may disappear when the remained charge is 40% in the investigated devices. Therefore, the retention time of sample A, 16 h, was obtained by means of extrapolating the curve I to where 40% charge was still stored. Similarly, the retention time of sample B was estimated to be 4580 h, which is three orders of the magnitude longer than the retention time of sample A. Apparently, a remarkable long-term retention time was achieved in sample B using dual memory nodes: nc-Si dots and traps of silicon–nitrides. For a comparison, an increase of two orders of magnitude was observed recently by R. Ohba in a doubly-stacked dots memory device [19].

It is notable that curve II can be fitted into two straight lines, the charge-loss rate of the first part (left-hand) is larger than that of the second part (right-hand), which implies that the discharging mechanisms are different for each of the linear parts [20]. As was aforementioned, the remaining and localized charges may be attributed to some of the charges falling into the traps of silicon–nitrides and failing to tunnel back directly to the channel because of the higher thermionic barrier. The difference of the charge-loss rate between samples A and B could be due to the difference of charge storage-sites: nc-Si dots for the former and nc-Si dots/traps for the latter. We suggest that the first discharge part of sample B may result from the electrons stored and delocalized entirely over the nc-Si dots, where the shorter distance from the channel and delocalized states may lead to a larger charge-loss rate, as what occurred in sample A. The discrepancy that the charge-loss rate of sample A is slightly greater than that of the first part (left-hand) of sample B may result from the larger number of electrons stored in the nc-Si dots compared to part of the stored electrons falling into nitride traps, thus, reducing the number of delocalized electrons. On the other hand, the second discharge part results from the localized charges in the nitride traps on top of the nc-Si dots, where the longer distance from the channel and localized states (thermionic barrier) leads to a smaller charge-loss rate.

In sample B, using dual memory nodes, a possible mechanism for write, store and erase programs may be explained as follows: in the write program, an electron in the channel might tunnel directly into the dot over the channel and the electron would be polarized to the top of the dot then localized in the trap at the top. This charge would be unable to tunnel back directly to the channel due to the long distance across the nc-Si dot as well as the thermionic emission barrier thus resulting in long-term retention times. With an applied erase gate bias, an erasure could be attained by thermionic emission from a trap at the top of the dot into delocalized state over the entire dot and tunnel back directly to the channel.

Since the utilized silicon–nitride films in the device are not the tunnel barrier but the memory nodes (located over the bottom nc-Si dots), carriers do not need transport across the nitride film and the Fowler–Nordheim tunneling or hot-electron effects are trivial. On the other hand, the ultathin thickness (1 nm) of silicon–nitride films also changes the injunction from the Fowler-Nordheim tunneling to the direct tunneling. Recent work pointed out that 256 000 programming erase-cycles using ± 8 V for 5 μs made no difference in the program/erase characteristics in the memory with similar structures and so presented the possibility of a DRAM with good cycling endurance [5]. Therefore, the programs of write and erase in the direct tunnel regime and discrete traps in the storage medium make this kind of devices to be an inherently high-reliability memory. However, further investigations are necessary to elucidate the mechanism of traps as well as their assisted charge/storage/discharge effects.

IV. Conclusion

The improved memory operations were demonstrated based on the dual memory nodes of nc-Si dots and traps in silicon–nitride films as memory floating-gates. The extra flat-band voltage shift in the *CV* characteristics can be attributed to the stored electrons falling into defect states of silicon–nitride

films and localized there. The smaller charge-loss rate was experimentally demonstrated in these kinds of memory devices compared to the memory devices using only nc-Si dots as floating-gates, which gave rise to a remarkable increase (three orders of the magnitude) of the memory retention time. Trap-assisted charging/discharging processes were suggested to generate a long-term retention time.

ACKNOWLEDGMENT

The authors would like to thank R. Nakamura for his assistance with SiO_2 deposition process and M. Kurosawa for his assistance with nitridation process.

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