Opto-electronic backplane for parallel computing

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Abstract: An optical backplane for multiprocessor computing is described. The architecture uses a fixed receiver path and implements a busy-bit protocol.

OCOCIS Codes: (200.4650) Optical interconnects, (999.9999) Multiprocessor interconnection networks

Optical interconnects can support a larger number of I/O [1][2] and can achieve higher bandwidths for less power than electrical interconnects [3][4][5][6]. Fixed receiver path networks (FRP-network), where each processor in the network has a unique receive path, reduce the complexity of on-chip data-path and control logic, as well as exploit the I/O count and bandwidth advantages of opto-electronics to increase the network bandwidth and to reduce node latencies. Fig. 1 shows the backplane components of a 64-processor FRP-network having 4 processors per processor board and 16 switch ICs providing the optical-to-electrical interface and network switching. With 8-bit wide datapaths, this network requires 512 (64x8) optical lines.

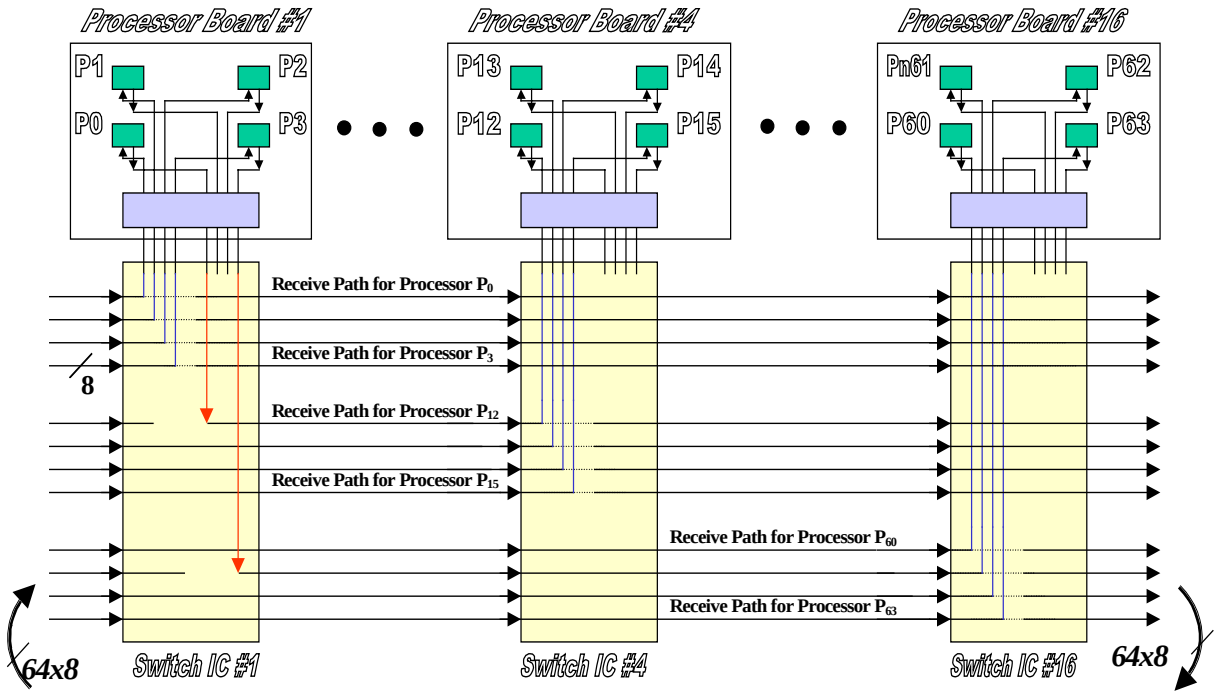

Fig. 1. Abstract of a 64 processor network, 4 processors per processor board, and 8-bit wide data paths requires 64x8 optical lines and 16 processor boards

In an FRP-network, a processor can only reach the destination processor through the destination's receive path and only if the destination is free. A "BUSY BIT" distributed path access protocol [7] is implemented in the backplane for path access arbitration. A global network clock is received from the reference processor board and is distributed optically to the remaining processor boards. The synchronization between the network clock and the processor board clock is performed at the processor board.

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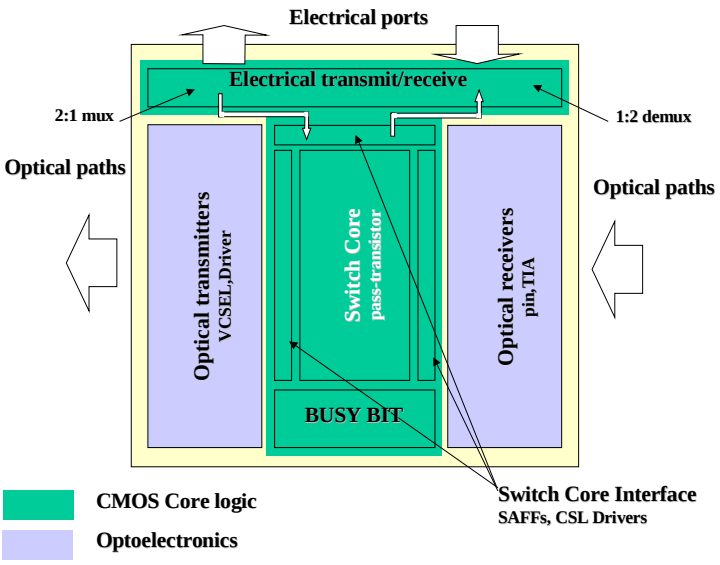

Fig. 2. Schematic of the CMOS switch IC. Backplane data flows right to left via an opto-electronic ring. Processors are attached via transmit/receiver ports.

The optical receive and transmit arrays of the opto-electronic switch IC are separated from the core logic and located on either side of the logic core as shown in Fig. 2. The optical inputs are received, 1:2 demuxed and retimed at the optical receivers, and are later retimed and 2:1 muxed at the optical transmitters. To reduce the clock load and power consumption, the switch core is implemented in complementary pass-transistor logic [8] and the electrical receivers, demux, mux, and the switch core interfaces use current-steering sense-amplifiers [9].

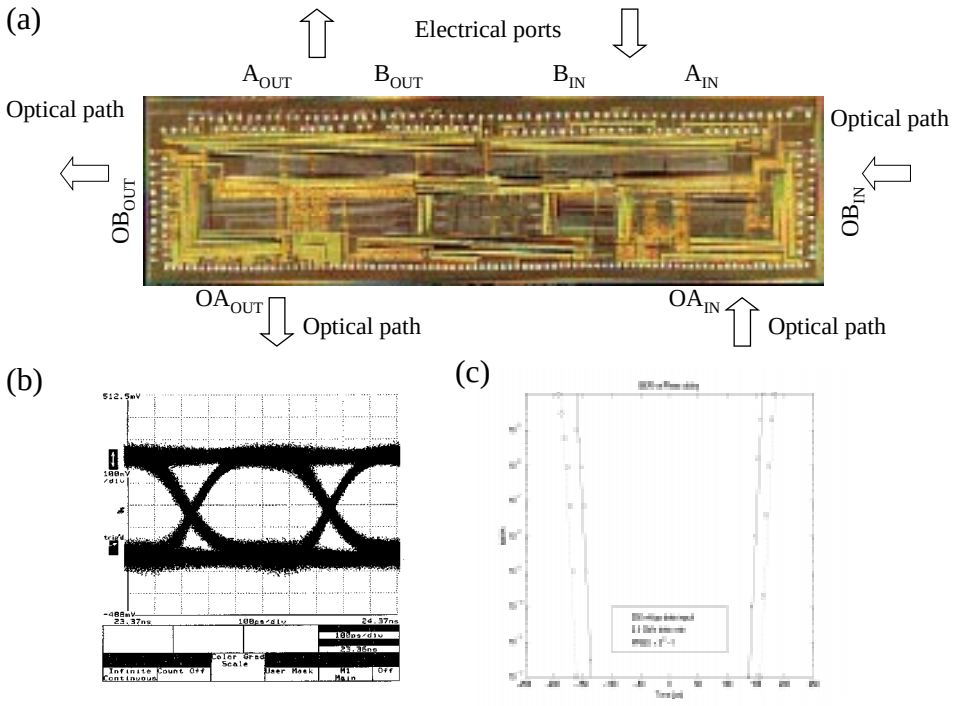

Fig. 3. (a) 32 Gb/s (2.0 Gb/s per line) , 4-Port TE02 test IC. Technology is 0.35 µm CMOS, power consumption 3.0 W, power rail 3.3 V, optical paths are OA and OB, electrical ports are A and B. (b) Measured eye diagram and (c) best and worst case phase margin at 2.0 Gb/s

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A 32 Gb/s (4 x 4x 2.0 Gb/s) 4-port switch IC was designed and tested in 0.35 μm CMOS technology (Fig. 3). At a data rate of 2.0 Gb/s, the IC had a worst case output phase margin of better than 55% at BER < 1 x 10^{-12} NRZ 2^{31}-1 PRBS. A scaled version of the IC, integrating both the CMOS and the optics, could support 64 processors at an interconnect bandwidth in the Tb/s regime (64x2x8). We are currently evaluating further scaling of the switch IC to support networks with greater than 64 processors and its use in hierarchically-connected fixed receiver path networks.

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