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ARTICLE

Strain-Insensitive, Air-Stable Stretchable Carbon Nanotube-Based Synaptic Transistors Array via Direct Microfabrication for Neuromorphic Computing

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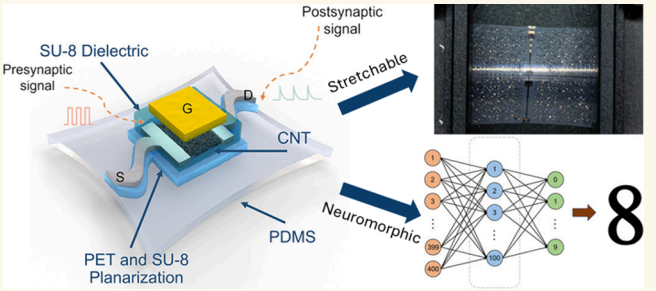
ABSTRACT: **Stretchable synaptic transistors show great promise in mimicking brain activities in soft robotics and skin electronics applications. However, the fabrication of such device arrays on elastic substrates with high stability, throughput, and yield remains challenging. Here, we have developed an approach to fabricate stretchable synaptic transistors directly on elastic substrates, in which carbon nanotubes and SU-8 are used as channel and dielectric, respectively. This method employs a fully photolithography-based microfabrication process that operates at relatively low temperatures. The devices exhibit an average on−off ratio of 2 × 10^6 and show minimal degradation when stretched up to 40%. Single-pulse, paired-pulse, and repetitive-pulse responses are also demonstrated, showing their ability to work as artificial synapses. The devices exhibit a high linearity of ≤1 with 100 distinct conductance states in long-term plasticity and a dynamic range of 15. Furthermore, we conducted a handwritten digit recognition simulation, achieving a learning accuracy of over 90%. We believe our work can serve as a guide for developing high-performance stretchable synaptic devices for various applications.**



KEYWORDS: *carbon nanotube, SU-8, stretchable electronics, microfabrication, synaptic transistor, neuromorphic computing*

INTRODUCTION

As Moore's law approaches its limit, traditional von Neumann computer architecture, which separates memory and processing units, faces limitations in energy efficiency and speed, making it inadequate for the emerging Internet of Things (IoT) era.[1] On the other hand, the nervous system is highly specialized and efficient in processing information and is of great referential significance for developing next-generation electronics.[2] Inspired by the biological nervous system, artificial synapses mimic the brain's architecture, enabling massive data storage and parallel data processing. This in-memory computing approach would be critical to address the von Neumann bottleneck.[3] Various two-terminal and three-terminal devices have been employed to build artificial synapses, including memristors,[4] transistors,[5] and photodetectors.[6] Compared with two-terminal structures, three-terminal structures offer superior synaptic stability, precise control over test parameters, and remarkable capability to realize transmission and learning functions, making them well-suited for neuromorphic computing applications.[7,8]

Notably, synapses in the biological nervous systems of humans and animals are usually soft and stretchable, enabling them to work under various mechanical stresses.[9] Developing stretchable artificial synapses that are similar to biological synapses is also of great importance for wearable sensory devices, neurological skin, and neuromorphic vision systems.[8,10−14] Stretchable synaptic transistors have been achieved with various organic materials due to their intrinsic softness, where "intrinsic" means the materials are capable of being deformed and returning to their original shape upon

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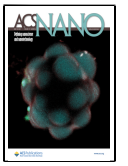

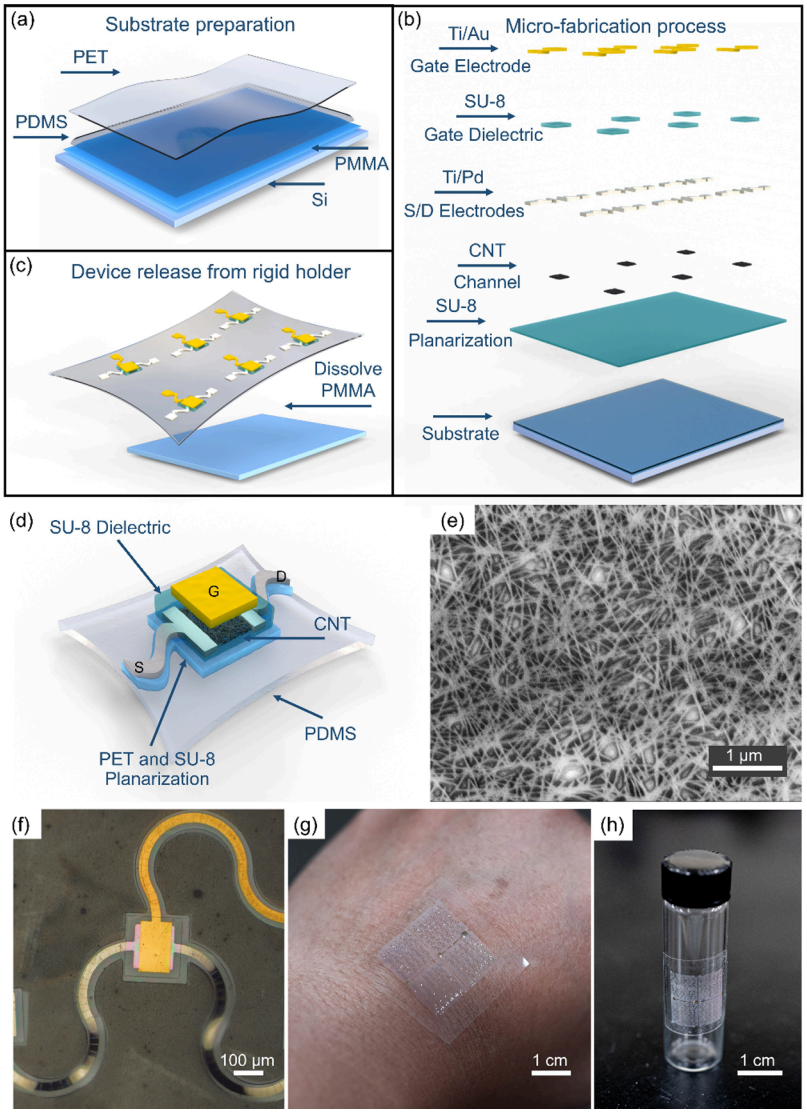

Figure 1. Fabrication process and images of the CNT-SSTs. (a) Substrate preparation. (b) Microfabrication process. (c) Release of devices from the rigid carrier. (d) Schematic of an as-fabricated device. (e) SEM image of the channel region of a device. (f) Optical microscopic image of one representative device. (g) Devices attached to human skin and (h) a curved surface.

release. For example, Yu et al. reported fully rubbery synaptic transistors made by all-organic materials using stencil mask and manual assembly, demonstrating an on−off ratio of 10^4, stretchability of up to 30%, and mobility of approximately 1.0 $cm^2/(V{\cdot}s)$.[15] However, the organic materials used in these devices may suffer from low mobility, thermal/chemical instability, and performance degradation under strain, resulting in challenges for applications and scalable production.[16,17] Compared to organic semiconductors, carbon nanotubes (CNTs) possess exceptional electrical and mechanical properties, high mobility, high current-carrying capacity, and intrinsic stretchability, making them an ideal option for flexible/stretchable electronics.[18−21] While nonstretchable CNT-based synaptic transistors have been previously demonstrated on rigid or flexible substrates,[5,7,22−24] stretchable CNT-based synaptic transistors have also stimulated great interest in recent years. For example, Bao et al. reported an inkjet printing method to produce intrinsically stretchable transistors with a channel length of 50 μm and a width of 1000 μm that operated under a 1 V, showing a 10^4 on−off ratio, 30 $cm^2/(V{\cdot}s)$ mobility, and up to 20% stretchability.[25] However, processing of intrinsically stretchable materials is usually not compatible with semiconductor microfabrication and instead requires inkjet printing, stencil mask patterning, or manual assembly, which is slow and produces devices with large feature sizes, thus limiting fabrication scalability and uniformity. So far, few studies have combined the following three important features into one platform regardless of the active channel material: semiconductor microfabrication techniques for scalability and high performance, stretchability for potential wearable electronics, and synaptic behavior for neuromorphic computing. The semiconductor fabrication approach can yield devices with superior electrical performance, remarkable uniformity, high-density integration, and outstanding stability, making it a promising approach for structurally stretchable electronics, where the stretchability is achieved via the structural design of interconnects, thus bypassing the constraint of using intrinsically stretchable materials with suboptimal electrical performance. Typically, the devices are fabricated on a polymer substrate (e.g., polyimide) carried by a rigid donor wafer.

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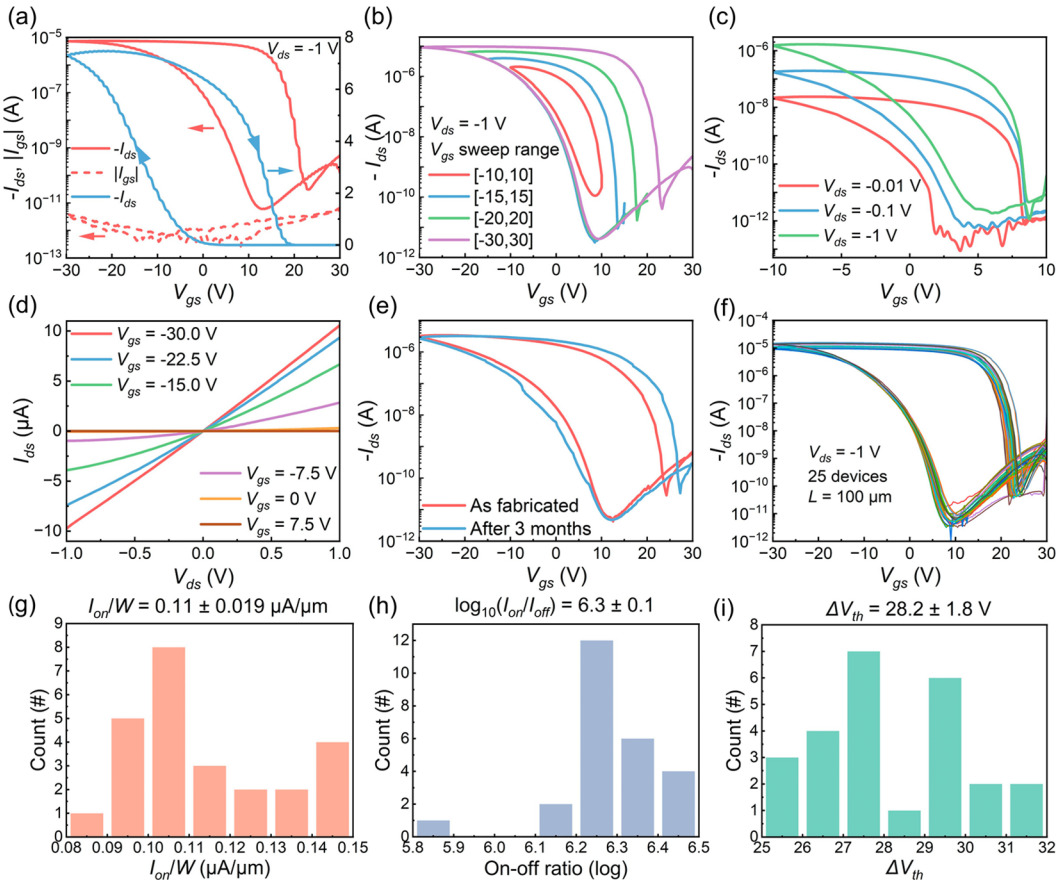

Figure 2. Electrical performance of CNT-SST without strain. (a) Transfer characteristic and gate leakage current of a representative device. Transfer characteristics under different (b) gate voltage sweep ranges. (c) Demonstration of reduced operation voltage using thinner SU-8 dielectric layer. (d) Output characteristics of a representative device. (e) Device measurements right after fabrication and after 3 months. (f) Cumulative transfer characteristics of 25 devices. Statistical distribution of the 25 devices in terms of (g) on-state current density, (h) on−off ratio, and (i) hysteresis window.

Inorganic electronic materials are patterned into wavy,[26] fractal,[27] or serpentine[28] geometries to accommodate the deformation in the systems and then transferred to an elastic substrate.[29,30] However, challenges still persist in achieving controllable synaptic behavior as it would require either charge-trapping layers or ferroelectric oxides, which involve complex multilayer fabrication or high-temperature processes and are often incompatible with stretchable substrates.

To our knowledge, few works have demonstrated structurally stretchable synaptic transistors via microfabrication techniques. Herein, we have developed a facile low-temperature approach to directly fabricate high-performance air-stable CNT stretchable synaptic transistors (CNT-SSTs) array on elastic substrates using fully photolithography-based microfabrication techniques, thus combining scalable microfabrication, stretchability, and synaptic behavior into one device platform. Specifically, serpentine-shaped metal interconnections were employed as the contacts, CNT network films were selected as the channel material, and SU-8 photoresist was used as the dielectric. The solution-processable nature of CNTs and the photopatternable characteristics of SU-8 dielectric facilitate easy microfabrication on a polydimethylsiloxane (PDMS) elastomer directly and limit the maximum process temperature below 110 °C (baking temperature). This direct fabrication method also eliminates the need for complex transfer printing steps in conventional microfabricated devices, reduces damage to devices, and further increases the yield.[31,32]

The synaptic behavior of CNT-SSTs results from the SU-8 dielectric, in which slow-moving mobile ions alter the postsynaptic current response. This hypothesis was confirmed by capacitance−voltage (C−V) measurements on CNT-SSTs. Moreover, the top-gated structures also serve as a passivation layer and play a vital role in preventing the CNT channel from exposure to species in the air. This results in significantly improved stability in ambient conditions when compared to CNT transistors with bottom gates where the CNT channel remains exposed to atmospheric species.[33] The devices exhibit an average on−off ratio of 2×10^6, as well as the ability to work below 10 V gate voltages and a low drain-to-source voltage of −0.01 V. They maintain constant performance under strain levels up to 30% and can fully regain their original properties when released from strains of 40%. Subsequently, we have also demonstrated programmable synaptic plasticity, including single-pulse, paired-pulse, repetitive-pulse response, and long/short-term plasticity. The devices show high linearity with 100 distinct conductance states and a dynamic range of 15. In addition, the device exhibited ultralow energy consumption, operating at just 1.05 fJ per pulse. Furthermore, a handwritten digit recognition simulation using NeuroSim 3.0 with the Modified National Institute of Standards and Technology (MNIST) dataset was conducted, and an accuracy of over 90% was achieved.[34,35]

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RESULTS AND DISCUSSION

The fabrication process of CNT-SSTs is summarized in Figure 1a−c. More detailed information on this process is provided in the Experimental Section and Supporting Information (Figure S1). The process started with substrate preparation, as shown in Figure 1a. Briefly, a stacked structure was prepared on a rigid holder wafer consisting of poly(methyl methacrylate) (PMMA), PDMS, polyethylene terephthalate (PET), and SU-8. Each layer served a specific purpose: PMMA acted as a sacrificial layer; PDMS functioned as an elastic substrate; PET minimized the thermal expansion effects of the PDMS elastomer and aided in subsequent microfabrication steps; and SU-8 acted as a planarization layer, smoothing the PET foil's surface and enhancing fabrication uniformity. Following the substrate preparation, top-gated CNT-SSTs were fabricated through conventional microfabrication, similar to our previous work, shown in Figure 1b.[19] It is worth mentioning that SU-8 was selected as the dielectric layer because (i) it can be processed at moderate temperatures, which enables the direct microfabrication process; (ii) it provides good mechanical/chemical stability, enabling a reliable operation under stretching/ambient; (iii) it is photopatternable, which reduces fabrication complexity; and (iv) it is inherent characteristics can lead to the synaptic behavior. After that, the PET was patterned into a serpentine shape by oxygen plasma to enable the devices to stretch. Finally, the devices were released from the carrier wafer by simply dissolving the PMMA sacrificial layer in acetone, as shown in Figure 1c; this release process introduces no strain to the devices, which reduces the possibility of device damage and further improves the yield. Figure 1d depicts a schematic of one device. The devices were fabricated with channel lengths (L) ranging from 100 to 5 μm while the channel width (W) is 100 μm. The 5 μm channel length represents the smallest feature size we successfully fabricated, while longer channels were fabricated as well for performance characterization. In addition, we have fabricated devices with 3 μm channel length, which exhibited low on−off ratio due to metallic CNTs directly bridging source and drain electrodes. Our subsequent analysis focuses on devices with channel lengths ranging from 100 to 5 μm. This photolithography-based fabrication method enables smaller feature sizes compared to printing and stencil mask techniques, which are typically limited to tens to hundreds of micrometers. Figure 1f is the scanning electron microscopy (SEM) image of the device channel region with CNT thin film. It shows that the CNTs are dispersed on the substrate uniformly as a network, with a density of approximately 20 tubes/μm^2. Figure 1e shows a microscope image of one representative device, and Figure 1g,h presents the photograph showing the device attached to human skin and a curved surface, demonstrating the potential of the devices working under different conditions.

To understand the working principle and evaluate the performance, a comprehensive electrical analysis of our CNT-SSTs was conducted. The electrical characterization was carried out after the devices were released from the rigid carrier without strain. We conducted measurements with different voltage sweep rates by varying the delay time from 0 to 1 s, which is the duration that the Keithley 4200 holds the bias before measuring each data point. As shown in Figure S2, the sweep rates affected the hysteresis to a certain degree but not significantly. For consistency, we maintained a zero-delay time setting for all other electrical measurements throughout this study. First, transfer characteristics of CNT-SSTs with channel lengths from 100 to 5 μm were measured at a fixed drain-to-source voltage (V_{ds}) of −1 V while sweeping the gate voltage (V_{gs}) from −30 to 30 V (Figure S3), and their performance metrics are compiled in Table S1. It can be concluded that the devices with 100 μm channel length are the best in terms of on−off ratio, hysteresis window, and operation voltage, thus potentially beneficial for neuromorphic applications. So, 100 μm devices were selected as representatives for further analysis. Figure 2a shows the dual-sweep transfer characteristics of a representative device with a L of 100 μm, a W of 100 μm, and under a V_{ds} of −1 V. The device shows typical p-type behavior as most other CNT-based devices, with a hysteresis window (different between the threshold voltage of two sweep branches, ΔV_{th}) of 28.2 V under V_{gs} sweep range from −30 to 30 V, an on−off ratio of approximately 10^6, and an ultralow gate leakage current of 10^{-12} A. The thickness of the SU-8 dielectric is 500 nm, and the specific capacitance is 5.3 nF/cm^2, as shown in Figures S4 and S5. The large hysteresis window, high on−off ratio, and low leakage are desirable to achieve high dynamic range and low power consumption for artificial synapses. Next, we investigated the hysteresis mechanism, which is essential for synaptic behavior. The hysteresis in CNT-based transistors is typically induced by charge-trapping,[18,22,23,36] ferroelectric,[7,37] or mobile ion mechanisms.[10,25,38] Notably, a clockwise hysteresis appears in the transfer characteristic of our CNT-SSTs, which is frequently reported in organic gate dielectric transistors due to polarized species within organic dielectric.[25,38] In our case, the hysteresis is caused by slow-moving ions.[39,40] In an SU-8 dielectric, ions are typically protons (H^+) and hexafluoroantimonate (SbF_6^-), which form when the photoacid generator within the SU-8 polymer is exposed to UV light during the photolithography process, causing the release of protons that then catalyze the cross-linking of epoxy groups.[41,42] Energy-dispersive X-ray spectroscopic (EDS) analysis, presented in Figure S6 and Table S2, confirms the presence of both Sb and F elements in the sample. As depicted in Figure S7, during a V_{gs} sweep from −30 to 30 V, these ions respond to the changing electric field. However, due to their finite mobility, they may lag behind these voltage changes. This delay means that when the voltage sweep is reversed, some ions may remain in their polarized positions rather than return to their initial states, creating a hysteresis effect. Therefore, the on-to-off swept transfer curve shifts to a higher V_{th} relative to the off-to-on swept one. To further verify the presence of ions in SU-8, we conducted a capacitance−voltage (C−V) dual sweep on a CNT-SST channel with the source and drain electrodes grounded as a metal−insulator-semiconductor (MIS) capacitor. Figure S8 shows a voltage shift in the C−V curves between forward and backward voltage sweeps. This shift is clear evidence of the presence of mobile ions.[43] This mechanism is also the origin of the synaptic behaviors, which will be discussed later. Figure 2b shows V_{gs} swept with different ranges under a constant V_{ds} of −1 V. The on−off ratio reached ~10^4 while the ΔV_{th} was around 10 V even when V_{gs} swept from −10 to 10 V, which is still sufficient for distinguishing conductance states in neuromorphic applications. It is evident that both the hysteresis window and the on−off ratio increased with increasing ΔV_{gs}. This gate-controlled transfer characteristic demonstrates the capability of programming multilevel conductance states for our CNT-SSTs. In applications where electronic devices are in direct contact with human skin, such

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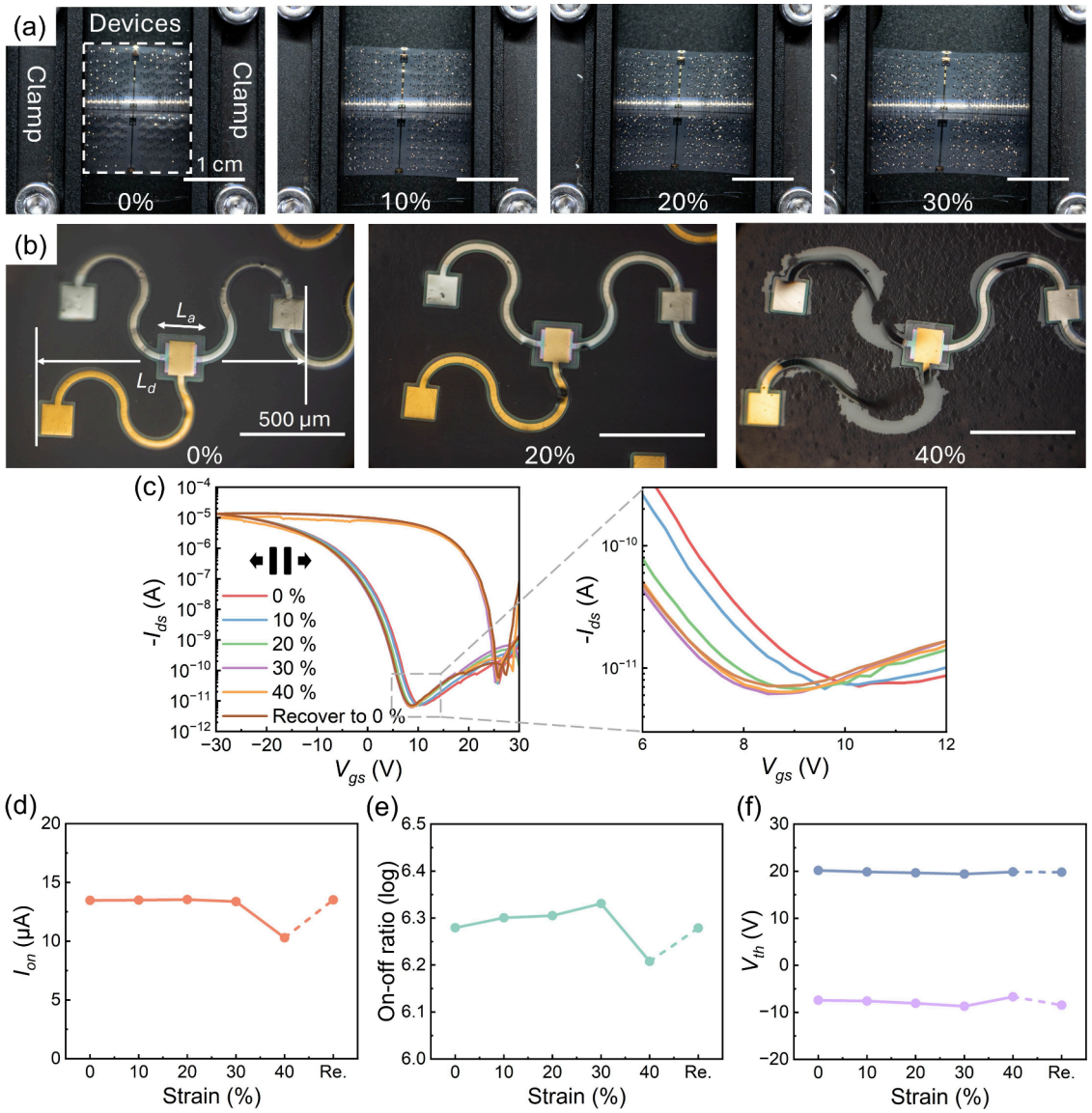

Figure 3. Electrical performance of the stretchable CNT synaptic transistor under strain. (a) Photograph of test fixture and CNT-SSTs under strain from 0 to 30%. (b) Microscope images showing devices under strain from 0 to 40%. (c) Transfer characteristics (and zoom in) of a representative device under strain from 0 to 40% and then recover to 0%. (d) Extracted on-state current, (e) on−off ratio, and (f) threshold voltage under strain from 0 to 40% and then recover to 0%.

as stretchable wearable technology, it is desirable to use lower voltages. Similarly, in neuromorphic computing systems, reducing these voltages helps minimize power consumption. Figure 2c shows CNT-SSTs with reduced SU-8 dielectric thickness, the transfer characteristic under V_{ds} from −0.01 to −1 V, and V_{gs} sweep from −10 to 10 V. The threshold voltage (V_{th}) remains nearly constant across these curves. As the $|V_{ds}|$ decreases from 1 to 0.01 V, there is a slight reduction in the on−off ratio, dropping from 10^6 to 10^5. This decrease occurs because, at lower $|V_{ds}|$ values, the off-state current approaches the same order of magnitude as the gate leakage current, creating a lower limit beyond which further reduction is not possible. This result ensures stable and robust operation under various working conditions and also demonstrates the potential of CNT-SSTs to operate at both low-voltage $|V_{ds}|$ and $|V_{gs}|$, making them suitable for wearable electronics applications. However, reducing the thickness resulted in lower fabrication yield and increased device-to-device variation. For the present study, we focused on devices with standard thickness. Then, the output characteristic measurement was carried out and exhibited in Figure 2d. The drain current increases considerably as the V_{gs} sweep from −30 to 30 V with an increment of 7.5 V, and a linear output characteristic is maintained. This indicates that good ohmic contacts were formed between the Pd electrodes and the CNT channel.[44,45] To confirm the stability of CNT-SSTs, a transfer characteristic was tested again after storing in ambient for three months, as shown in Figure 2e. The on- and off-state currents stayed almost identical, while V_{th} has slightly changed. Moreover, to understand the stability of CNT-SSTs under harsh environmental conditions, particularly under prolonged exposure to light, we have conducted exposure tests using a solar simulator at 100 mW/cm^2, which matches typical solar illumination intensity. Transfer characteristics were measured at multiple time points of solar exposure. As shown in Figure S9, the devices maintained reliable operation after 500 h of exposure.

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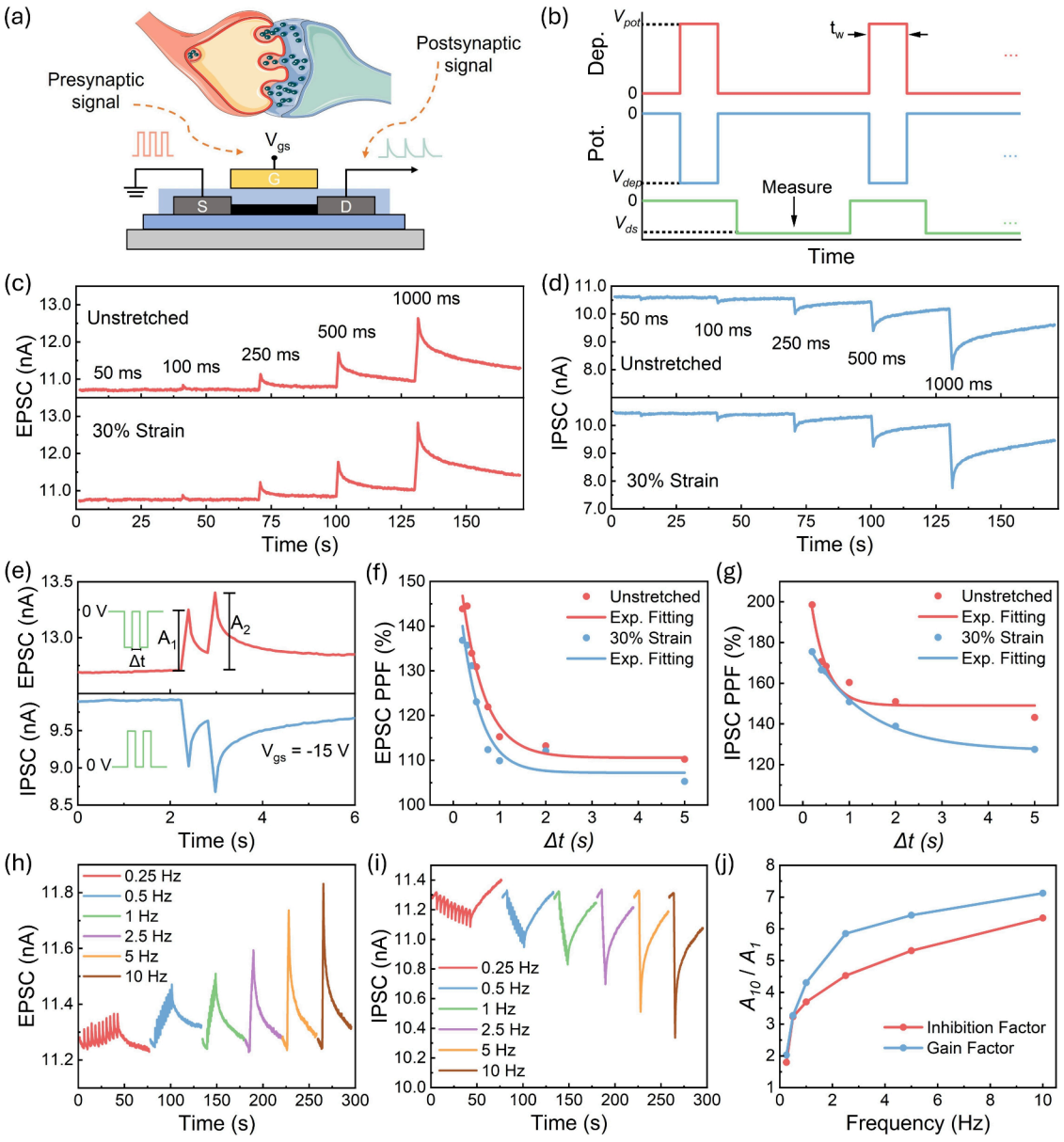

Figure 4. Pulse response of a stretchable CNT synaptic transistor. (a) Schematic diagram of the biological synapse and artificial CNT-SST for mimicking biological synaptic behavior. (b) Schematic of the EPSC and IPSE measurement methods. (c, d) EPSC and IPSC of the device in response to pulse width under 0 strain and 30% strain. (e) Concept of paired-pulse facilitation (PPF). (f, g) EPSC and IPSC PPF of the CNT-SST under 0 and 30% strain. (h, i) Synaptic plasticity EPSC and IPSC in response to the stimulus train at different frequencies. (j) Gain/inhibition factor of the EPSC/IPSC (A_{10}/A_1) with respect to different pulse frequencies.

While there were slight changes in performance—specifically, a small increase in the on-state current and a reduction in the hysteresis window—these variations remained within acceptable operational limits.

To evaluate the yield and uniformity of the devices, we conducted a cumulative test of 26 identical devices on the same substrate. Of these, 25 devices functioned correctly, resulting in a 96% yield rate. Figure 2f exhibits the transfer characteristics of these devices, showing a high device-to-device uniformity. We further validated this result by statistical analysis of device parameters extracted from the curves. Figure 2g–i shows the distribution of on-state current density (I_{on}/W), on–off ratio, and hysteresis window. The analysis revealed an average on-state current density of 0.11 ± 0.019 μA/μm, $\log(I_{on}/I_{off})$ of 6.3 ± 0.1 (on–off ratio of 2.0 × 10^6), and a hysteresis window of 28.2 ± 1.8 V. The spatial distribution map of on-state current is presented in Figure S10, demonstrating high uniformity across the substrate. Moreover, we analyzed device performance across three separate production batches, with results shown in Figure S11 and Table S3. The consistently high performance across multiple batches demonstrates the reproducibility of our fabrication process and validates the reliability of CNT-SSTs.

Microscopic and electrical characterization under strain was then carried out to evaluate the stretchability of CNT-SSTs. Figure 3a shows a photograph of CNT-SSTs being stretched from 0 to 30% using a stretching device; the devices are fixed by two clamps on both sides, and the rod beneath the devices is a worm that enables the movement of the clamps and thus stretches the devices. Optical microscopic images of a single

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device under varying strain levels, from 0 to 40%, were analyzed to reveal the mechanical properties under strain, as shown in Figure 3b. We defined L_a as the length of the active region and L_d as the total length of the device. At 0% strain, L_a measured 240 μm, while L_d was 1200 μm. Upon applying 20 and 40% strain, we observed that L_a remained constant at 240 μm, whereas L_d increased to 1440 and 1680 μm, respectively. These measurements demonstrated that CNT-SSTs are structurally stretchable devices, with the serpentine interconnections accommodating most of the strain while the deformation on the active region is minimal. Interestingly, as depicted in Figure 3b, under high strain (40%), the serpentine interconnections detached from the substrate to accommodate the deformation, and they reattached to the substrate upon release without structural damage, as confirmed by both optical and SEM imaging (Figures S12 and S13).

Unlike intrinsically stretchable devices that show performance change when stretched,[25,38,46] our CNT-SSTs maintain stable performance even under high mechanical stress. Figure 3c displays the transfer characteristics of a typical device under strain from 0% to 40%, including a magnified view of the data. Figure 3d−g illustrates the key metrics extracted from the transfer characteristics: on-state current density, on−off ratio, and threshold voltage. These parameters remain highly stable under strains ranging from 0 to 30%, demonstrating the CNT-SSTs' excellent strain insensitivity. At 40% strain, there is a 20% decrease in on-state current, causing a slight reduction in the on−off ratio. However, upon returning to 0% strain, the device performance fully recovers, highlighting the stability of CNT-SSTs. To evaluate the device's durability, we performed cyclic strain testing. Figure S14 demonstrates that the device performance does not notably change even after 1000 strain cycles of strain up to 30%. The devices maintain high performance under strain because both the active regions and interconnections remain structurally intact during stretching. SEM imaging (Figure S13) reveals that there are no cracks developed under strain; the visible traces on the serpentine interconnections are merely creases in the underlying PET substrate rather than microcracks in the interconnections themselves.

In a biological synapse, the presynaptic terminal communicates with the postsynaptic terminal by modulating the release of different neurotransmitters, generating either excitatory or inhibitory signals. Synapses regulate the propagation of action potential between neurons, facilitate the transmission of information across neurons, and determine the synaptic strength or weight, thus ultimately governing learning and memory formation within the biological system. A three-terminal synaptic transistor and biochemical synapse have certain similarities, allowing us to utilize the properties of our devices to mimic biological synapses (Figure 4a). Basically, the presynaptic and postsynaptic terminals are represented by gate and drain terminals. Electrical pulses applied to the gate terminal serve as stimulation for the presynaptic terminal. Since the dielectric of CNT-SSTs operates based on the "slow-moving species" mechanism, an excitatory postsynaptic signal is produced when the gate terminal receives a negative potentiation pulse (V_{pot}). Conversely, an inhibitory postsynaptic signal arises from a positive depression pulse (V_{dep}). To measure the postsynaptic signal, a small drain-to-source bias (V_{ds}) is then applied to measure the drain current, as shown in Figure 4b.[23]

The single pulse-induced excitatory postsynaptic current (EPSC) and inhibitory postsynaptic current (IPSC) were tested under ± 15 V presynaptic voltage with different pulse widths (t_w) ranging from 50 to 1000 ms, and V_{ds} of −10 mV were employed for postsynaptic current measurements. The results are shown in Figure 4c,d; as t_w increases, both ΔEPSC and ΔIPSC increase. This behavior is due to increased polarized ions density within the SU-8 dielectric with longer t_w. The EPSC retention time varied from 400 ms to 16 s when the presynaptic pulse width was adjusted between 50 and 1000 ms. This demonstrates that synaptic plasticity can be controlled by modulating the duration of presynaptic pulses.[22] The CNT-SST remained functional when operated at a lower presynaptic voltage of ±5 V, though this resulted in reduced response amplitude, as shown in Figure S15. It is also noticeable that the pulse response of ΔIPSC and ΔEPSC under 30% strain is almost the same as without strain, which proves the strain insensitivity. The devices also demonstrated mechanical durability, maintaining both EPSC and IPSC performance after 1000 cycles of 30% strain, as shown in Figure S16.

We have further studied the EPSC and IPSC triggered by two successive presynaptic pulses. The paired-pulse facilitation (PPF) index is defined as the ratio of the second EPSC peak (A_2) over the first one (A_1), denoted as $A_2/A_1 \times 100\%$. PPF reflects short-term synaptic plasticity and can be modulated by changing the interval (Δt) between two pulses[15,37] (Figure 4e). The PPF index with respect to Δt of both EPSC and IPSC are plotted in Figure 4f,g. The PPF index of EPSC is 145% without strain and 137% with 30% strain, while it is 198% without strain and 177% with 30% strain for IPSC. The PPF decreases exponentially when Δt increases from 250 ms to 5 s. The PPF index of EPSC is generally lower than that of IPSC, suggesting that the potentiation response is weaker than the depression response. This is due to the asymmetric hysteresis in the transfer characteristics and depletion working mode of our CNT-SSTs; when a positive depression presynaptic pulse is applied, the postsynaptic current changes faster than when a negative potentiation pulse is applied.[11]

The filtering characteristics of biological synapses are essential for the transmission of signals in the nervous system.[4] In some synapses, high-frequency stimuli are needed for presynapse to release neurotransmitters, so they work as high-pass filters. We explored the synaptic filtering properties of our devices by applying ten successive presynaptic pulses of ±15 V with frequencies from 0.25 to 10 Hz, which led to a reduction in the time interval between spikes, shown in Figure 4h,i. It can be clearly seen that both EPSC and IPSC have weak responses to low frequencies; after the pulses end, the postsynaptic current recovers to the original level immediately, while the response is enhanced when the frequency goes higher. This means our CNT-SSTs are working as high-pass filters. The gain/inhibition factors of frequency filtering for EPSC and IPSC are defined as A_{10}/A_1, which are extracted from the measurement in Figure 4g,h and depicted in Figure 4j. The gain/inhibition factor at 0.25 Hz are 1.90 and 2.05 and increase to 6.10 and 7.10 as frequency increases to 10 Hz.

In addition, the power consumption of artificial synaptic transistors is a key parameter. Since biological synapses consume only 1−100 fJ of energy, it is worthwhile to reduce the power consumption of artificial synaptic devices.[8,47] The power consumption of synaptic transistors can be expressed using the following equation:[48]

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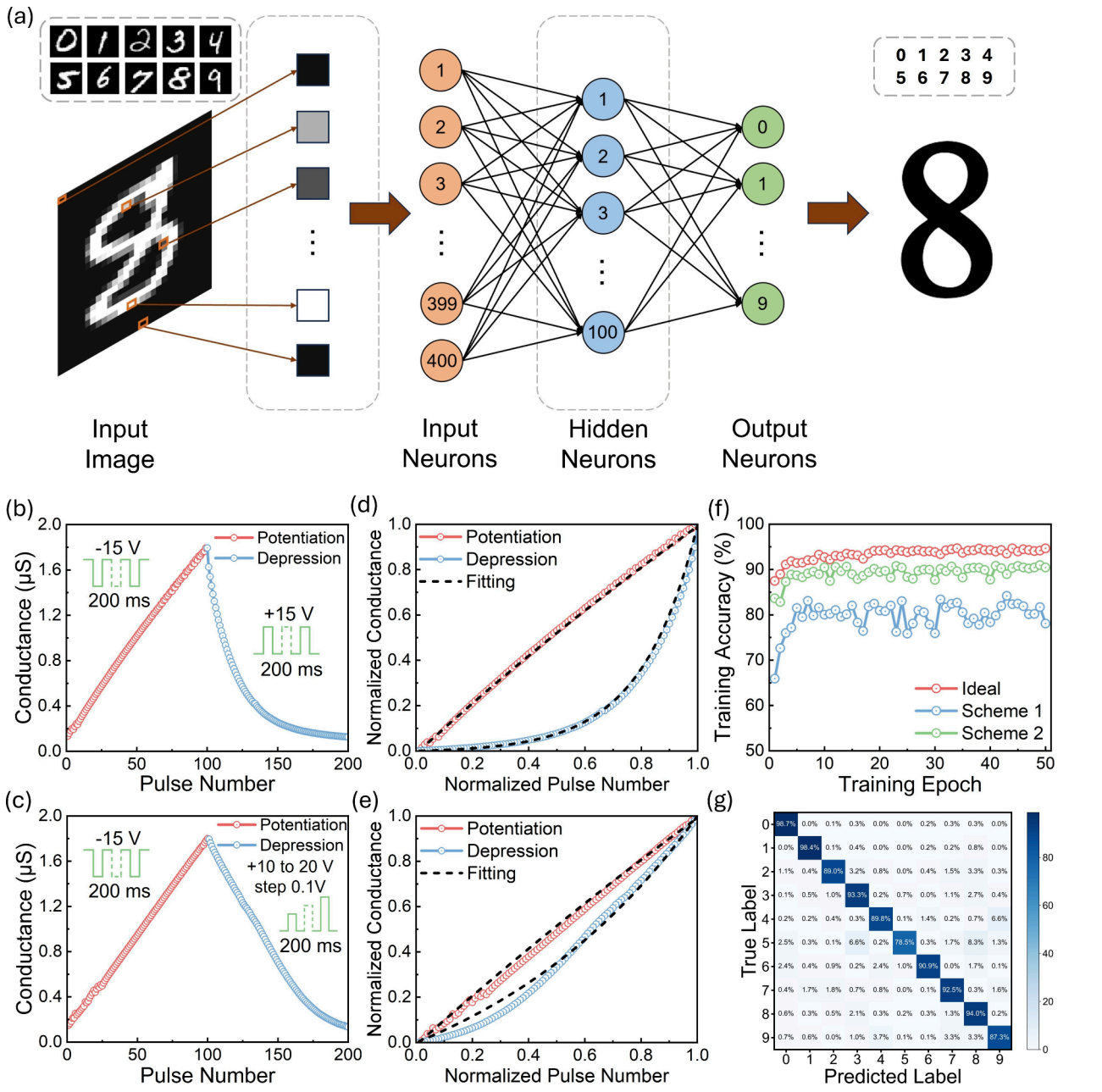

Figure 5. Pattern recognition simulation with the CNT-SSTs. (a) Schematic illustration of a three-layer neural network for handwritten digit recognition. (b, c) Conductance changes with respect to pulse number during potentiation and depression, and (d, e) nonlinear fittings of normalized conductance plots for different pulse configurations. (f) Pattern recognition simulation result of ideal case, pulse scheme 1 and scheme 2. (g) Confusion matrix from training epoch 50 of scheme 2.

$$E = V_{ds} \times I_{peak} \times t_w$$

where V_{ds}, I_{peak}, and t_w represent the reading drain voltage, EPSC peak current, and pulse width, respectively. The power consumption was calculated to be 1.05 fJ, under a V_{ds} of 1×10^{-5} V and a t_w of 50 ms (Figure S17). This suggests that our CNT-SSTs have ultralow power consumption compared to other existing synaptic transistors.[22,38,45,46,48]

We further explored the potential applications of our devices in neuromorphic computing, and a simulation on handwritten character recognition was subsequently conducted. NeuroSim 3.0 framework was employed to benchmark the performance of our devices. Specifically, these devices were used as artificial synapses in an artificial neural network (ANN) for recognition using the MNIST handwritten dataset. The MNIST dataset consisted of 60,000 training images and 10,000 testing images. For our simulations, we used NeuroSim 3.0's default network settings, as illustrated in Figure 5a. The network consists of three layers: an input layer with 400 neurons representing image pixels, a hidden layer with 100 neurons, and an output layer with 10 neurons corresponding to digits 0 through 9. Using these standard settings enables direct comparison with other studies that employ the same framework, ensuring consistent testing conditions for reliable benchmarking.

Long-term plasticity (LTP) under different pulse profiles was studied to obtain the parameters needed for the simulation. Figure 5b shows 100 identical consecutive pulses with ±15 V and 200 ms pulse width were applied as a

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presynaptic signal, and the postsynaptic current was measured using the method mentioned in Figure 4b under V_{ds} of −0.01 V. Then, the dynamic range and nonlinearity properties were analyzed. The conductance was first normalized and processed to get Figure 5d (details in Estimation of Nonlinearity from the Supporting Information) and then fitted using the following model:

$$G_{LTP} = B(1 - e^{-P/A}) + G_{min}$$

$$G_{LTD} = -B(1 - e^{P-P_{max}/A}) + G_{max}$$

$$B = \frac{G_{max} - G_{min}}{1 - e^{-P_{max}/A}}$$

G_{LTP} and G_{LTD} are conductance for long-term potentiation (LTP) and long-term depression (LTD). G_{max} and G_{min} denote the maximum and minimum conductance; P and P_{max} indicate the pulse number and maximum pulse, respectively. In our case, P is a number from 1 to 100, and P_{max} is 100, which represents the number of effective conductance states. A is the parameter that controls the nonlinear behavior of weight update, which is extracted from fitting.[49] Moreover, the dynamic range is defined as the ratio of maximum conductance to minimum conductance (G_{max}/G_{min}); the nonlinearity (NL) of the curve can be converted from the parameter A in the fitting formulas. In the scheme depicted in Figure 5b, the G_{max} and G_{min} are 0.12 and 1.8 μS, giving a dynamic range (DR) of 15. The NL of potentiation and depression are 0.3 and 4.0. The simulation result is plotted in Figure 5f, and an average accuracy of 80% is achieved. According to Chen and Yu, nonlinearity $\leq$ 1, number of conductance states $\geq$ 64, and dynamic range $\geq$ 10 are required to achieve reasonably good accuracy.[50] To further promote the performance, we employed a stepped presynaptic pulse profile to reduce the NL of the LTP. Specifically, for potentiation operations, the pulse voltage was constant −15 V with a 200 ms pulse width, which was the same as the previous scheme. For depression operations, the pulse voltage increased from 10 to 20 V with a step of 0.1 V as the pulse number increased from 1 to 100. The result is plotted in Figure 5c,e; an NL of 0.3 and 1.0 is observed for potentiation and depression, while the NL of depression shows a significant decrease. The DR remains the same in both scenarios. This improved NL led to a higher accuracy of 90%, as shown in Figure 5f. The ideal case simulation was also conducted with the same dynamic range and without nonlinearity, i.e., DR = 15 and NL = 0. The accuracy of 93% is slightly higher than the result of using real devices, demonstrating the excellent performance of our devices. Figure 5g presents a confusion matrix from the 50th training epoch of scheme 2, where each element represents the percentage of instances for which a true label was assigned a particular predicted label. The prominent diagonal values in the matrix demonstrate that the predicted classifications closely match the true labels across all pattern recognition tasks, indicating high classification accuracy.

CONCLUSIONS

In conclusion, we have developed a facile low-temperature method to fabricate CNT stretchable synaptic transistors on an elastic substrate directly. The devices exhibit an on−off ratio of 2×10^6, high uniformity, and ambient stability. They operate at gate voltages below 10 V and a low drain-to-source voltage of −0.01 V. The devices also show strain tolerance, maintaining consistent performance under deformations of up to 30%. A maximum stretchability of 40% is achieved with minimal degradation in performance, and the performance fully recovers once the strain is removed. We applied the devices for neuromorphic applications; EPSC and IPSC were first tested, showing the potential for mimicking human neural systems. A 1.05 fJ ultralow single pulse power consumption was also obtained. Subsequently, pattern recognition simulation was conducted and demonstrated a dynamic range of 15 and a low nonlinearity of 0.3 and −1.0 for potentiation and depression, respectively. A 90% accuracy in online learning was achieved. Our work has demonstrated a possible new method for the facile and scalable fabrication of high-performance stretchable synaptic devices, paving the way for the development of next-generation wearable electronics and biointegrated neural interfaces.

EXPERIMENTAL SECTION

Preparation of Elastic Substrate. First, a layer of poly(methyl methacrylate) (PMMA) was spin-coated onto a silicon wafer. Subsequently, polydimethylsiloxane (PDMS, SYLGARD184, with a base-to-curing agent ratio of 10:1) was spin-coated at 500 rpm and cured in an oven at 75 °C for 4 h. A 3 μm-thick polyethylene terephthalate (PET) foil was then laminated onto the elastomer. Finally, SU-8 2000.5 was spin-coated onto the PET foil and cross-linked by ultraviolet (UV) flood exposure to work as a planarization layer.

CNT Film Deposition. The CNT film was deposited using an incubation method reported previously.[19] Initially, a 0.1% (v/w) poly-L-lysine solution was drop-cast onto the substrate and left for 10 min, followed by deionized (DI) water rinsing and nitrogen blow-drying. Subsequently, 0.01 mg/mL CNT in toluene solution (IsoSol-S100, NanoIntegris) was drop-cast onto the substrate and incubated for 15 min, followed by toluene rinsing and nitrogen blow-drying. Finally, the substrate with the CNT film was baked in air at 90 °C on a hot plate for 30 min.

Stretchable CNT Synaptic Transistor Fabrication. The CNT devices were fabricated using typical microfabrication processes. First, a bilayer of 3 nm titanium and 50 nm palladium films was patterned as the source and drain electrodes via photolithography, electron beam deposition, and a lift-off process. Next, unwanted CNT film outside the channel region was removed by an oxygen plasma treatment (Oxford 80, 100 W, 150 mTorr, and 30 s), with 1.5 μm AZ 5214 as the etching mask. Subsequently, a 500 nm-thick layer of SU-8 2000.5 was spin-coated and photopatterned as the dielectric layer. Then, a bilayer of 3 nm titanium and 50 nm gold was defined as the top gate electrode. To enable device stretchability, the SU-8/PET layers outside the active region and serpentine interconnections were removed.[16] Specifically, the desired region was first covered by patterned AZ P4620 photoresist (12 μm thick). This photoresist layer acted as an etching mask. Then, the uncovered SU-8/PET areas were etched away with oxygen plasma treatment (Oxford 80, 250 W, 100 mTorr, and 5 min), preserving only the active region and serpentine interconnections that were protected. Finally, the PMMA sacrificial layer was dissolved in acetone, releasing the stretchable device from the rigid carrier.

Materials and Device Characterization. The SEM and EDS studies were performed using a Nova NanoSEM 450 field-emission scanning electron microscope. The thickness of the SU-8 dielectric was measured using DektakXT profilometer. Electrical characteristics of the CNT-SSTs were conducted with a Keithley 4200-SCS semiconductor characterization system associated with the pulse measurement unit (PMU), capacitance−voltage unit (CVU), and source measurement units (SMUs).

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ASSOCIATED CONTENT

Supporting Information

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Additional figures and tables that enhance understanding of CNT-SSTs: fabrication flowchart, summary of channel length dependent metrics, EDS analysis of SU-8, schematic to explain slow-moving ions mechanism, distribution map of on-state current, performance statistics of multiple devices from different batches, optical microscope and SEM images of CNT-SSTs, durability of both transistor and synaptic performance under repeated stretching cycles, synaptic responses under lower presynaptic voltage, EPSC and IPSC of a single pulse under V_{ds} = 1 × 10^{-5} V, estimation of nonlinearity, and comparison with state-of-art stretchable synaptic transistors (PDF)

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Notes

The authors declare no competing financial interest.

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