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ARTICLE

High-Performance Sub-Micrometer Channel WSe_2 Field-Effect Transistors Prepared Using a Flood−Dike Printing Method

Fanqi Wu,[†,□] Liang Chen,[‡,□] Anyi Zhang,[†] Yi-Lun Hong,[§,∥] Nai-Yun Shih,[†] Seong-Yong Cho,[⊥] Gryphon A. Drake,[⊥] Tyler Fleetham,[#] Sen Cong,[‡] Xuan Cao,[†] Qingzhou Liu,[†] Yihang Liu,[‡] Chi Xu,[¶] Yuqiang Ma,[¶] Moonsub Shim,[⊥] Mark E. Thompson,[#] Wencai Ren,[§] Hui-Ming Cheng,[§] and Chongwu Zhou*[,†,‡]

[†]Department of Chemical Engineering & Materials Science, [‡]Department of Electrical Engineering, [#]Department of Chemistry, and [¶]Department of Physics & Astronomy, University of Southern California, Los Angeles, California 90089, United States

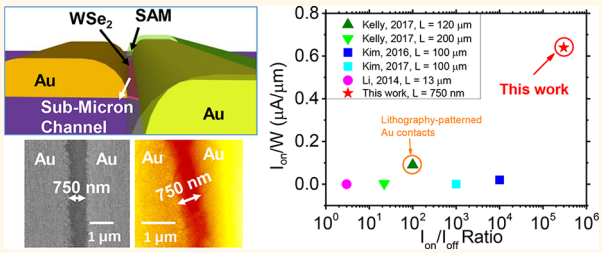
[§]Shenyang National Laboratory for Materials Science, Institute of Metal Research, Chinese Academy of Sciences, Shenyang 110016, People's Republic of China

[∥]School of Materials Science and Engineering, University of Science and Technology of China, 72 Wenhua Road, Shenyang 110016, People's Republic of China

[⊥]Department of Materials Science and Engineering and Materials Research Laboratory, University of Illinois, Urbana, Illinois 61801, United States

Supporting Information

ABSTRACT: Printing technology has potential to offer a cost-effective and scalable way to fabricate electronic devices based on two-dimensional (2D) transition metal dichalcogenides (TMDCs). However, limited by the registration accuracy and resolution of printing, the previously reported printed TMDC field-effect transistors (FETs) have relatively long channel lengths (13−200 μm), thus suffering low current-driving capabilities (≤0.02 μA/μm). Here, we report a "flood−dike" self-aligned printing technique that allows the formation of source/drain metal contacts on TMDC materials with sub-micrometer channel lengths in a reliable way. This self-aligned printing technique involves three steps: (i) printing of gold ink on a WSe_2 flake to form the first gold electrode, (ii) modifying the surface of the first gold electrode with a self-assembled monolayer (SAM) to lower the surface tension and render the surface hydrophobic, and (iii) printing of gold ink close to the SAM-treated first electrode at a certain distance. During the third step, the gold ink would first spread toward the edge of the first electrode and then get stopped by the hydrophobic SAM coating, ending up forming a sub-micrometer channel. With this printing technique, we have successfully downscaled the channel length to ∼750 nm and achieved enhanced on-state current densities of ∼0.64 μA/μm (average) and high on/off current ratios of ∼3 × 10^5 (average). Furthermore, with our high-performance printed WSe_2 FETs, driving capabilities for quantum-dot light-emitting diodes (LEDs), inorganic LEDs, and organic LEDs have been demonstrated, which reveals the potential of using printed TMDC electronics for display backplane applications.



KEYWORDS: *tungsten diselenides, transition metal dichalcogenides, TMDC, two-dimensional, chemical vapor deposition, printing, sub-micrometer channel*

Transition metal dichalcogenides (TMDCs), which are two-dimensional (2D) layered materials, generally have a formula of MX_2, where M stands for a transition metal and X stands for a chalcogen.[1−3] Depending on the composition, the TMDCs can span from superconductors to semiconductors and even insulators[1,4,5] Meanwhile, other factors including thickness, defects, and strain can also affect their physical properties such as band gap and field-effect mobility.[6−10] Among the large family of TMDCs, MoS_2 and WSe_2 are the two most widely studied species, with interesting semiconducting features.[11−13] In particular, monolayer WSe_2, which possesses a direct band gap and ambipolar transport

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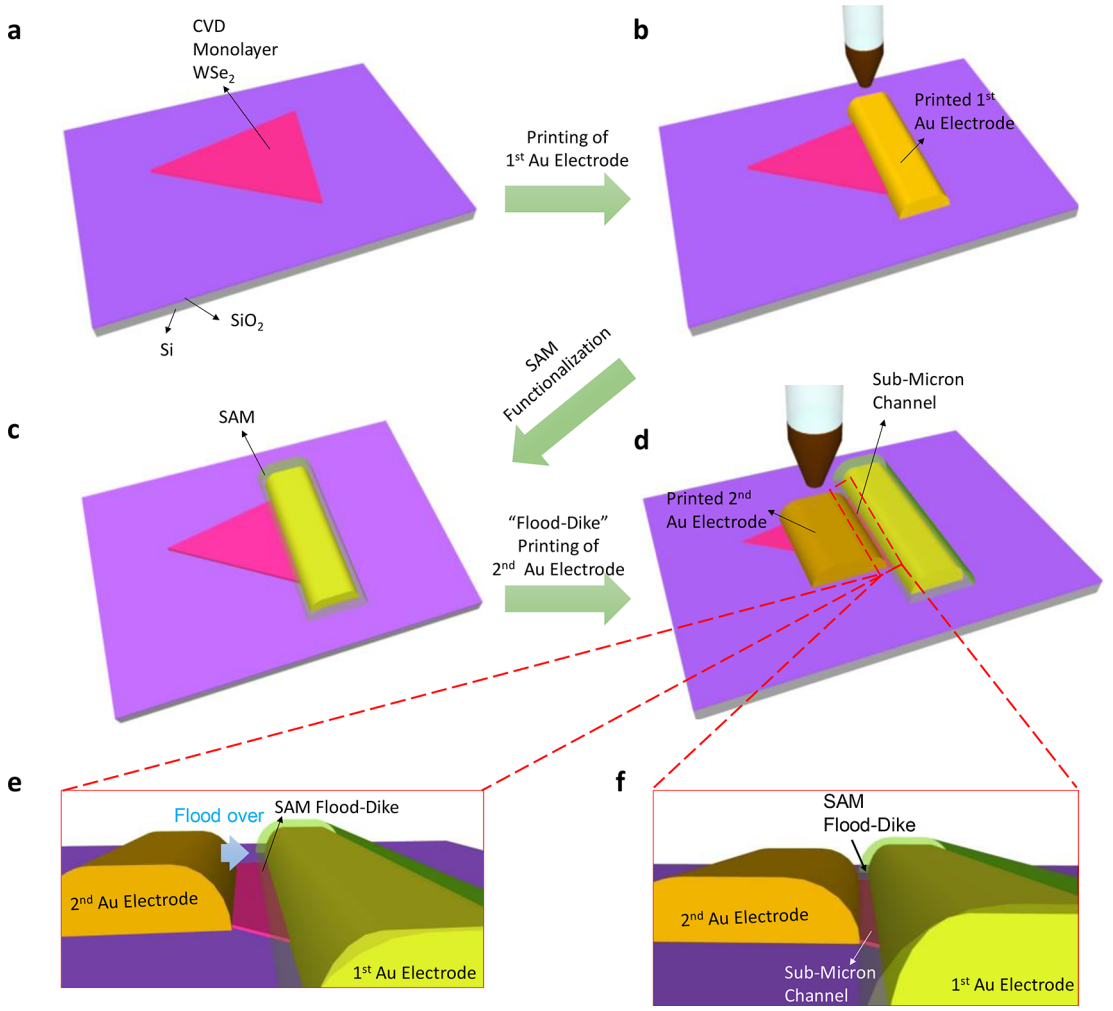

Figure 1. "Flood–dike" self-aligned printing of short-channel FETs based on CVD WSe_2. (a) Schematic diagram showing a single-monolayer triangle-shape WSe_2 flake transferred on Si/SiO_2. (b–d) Schematic diagrams showing the three steps of the "flood–dike" self-aligned printing method, including (b) printing of the first gold electrode, (c) functionalizing the surface of the first electrode with SAM, and (d) printing of the second gold electrode close to the first one. (e) Zoomed-in schematic diagram showing the gold ink of the second electrode flooding toward the first electrode right after landing on the WSe_2 surface. (f) Zoomed-in schematic diagram showing the gold ink gets stopped by the SAM "flood–dike", forming a short channel on the sub-micrometer scale.

behavior,[14,15] has been demonstrated as a good candidate for optoelectronics,[16−19] spintronics,[20] and valleytronics.[13,21] At the same time, this TMDC material is also suitable for other electronic applications such as chemical sensing and flexible electronics because of the 2D layered nature.[22−25]

In another aspect, current semiconductor manufacturing relies heavily on sophisticated fabrication processes such as lithography and vacuum deposition, which may be prohibitively costly and time-consuming to adapt to TMDC-based devices. Fortunately, printing technology designed for solution-based low-temperature processing can eliminate the needs for high-cost lithography and vacuum systems.[26] Up to now, printing approaches have been reported for a number of devices including field-effect transistors (FETs), logic gates, and solar cells using carbon nanotubes (CNTs),[27−33] metal oxides,[33−35] organic films,[36,37] or inorganic nanoparticles,[38] which demonstrate the great potential of using printing technology for low-cost and large-scale electronic applications.[39−41] Recently, significant progress has been made in printed electronics based on 2D TMDCs.[42−46] In 2014, Li *et al.* demonstrated fully inkjet-printed MoS_2 FETs by printing MoS_2 liquid dispersions on top of printed silver contacts.[44] Later on, Kim *et al.* reported chemical vapor deposition (CVD)-synthesized monolayer MoS_2 FETs with inkjet-printed silver contacts.[43] Recently, a family of liquid-exfoliated TMDC nanosheet inks have been utilized for all-printed FETs by Kelly *et al.*[45] and all-printed photodetectors and memory devices by McManus *et al.*,[47] respectively. Nevertheless, previously reported printed 2D TMDC devices usually have rather long channel lengths on the scale of 13 μm–200 μm, mainly limited by the resolution and the registration accuracy of the printing instrument. A large channel length would compromise the device performance, especially the on-state current density, resulting in a relatively low current-drive capacity ($\leq$0.02 $\mu A/\mu m$). A major reason is that, within such a long channel length, there exists a large number of either flake-to-flake junctions (for liquid-exfoliated TMDC nanosheet networks) or grain boundaries (for continuous TMDC films). Therefore, downscaling of the transistor channel length is desired to improve the device performance and enable potential applications.

Previously, Sirringhaus *et al.* reported a back-contact self-aligned printing method for sub-micrometer FETs with organic

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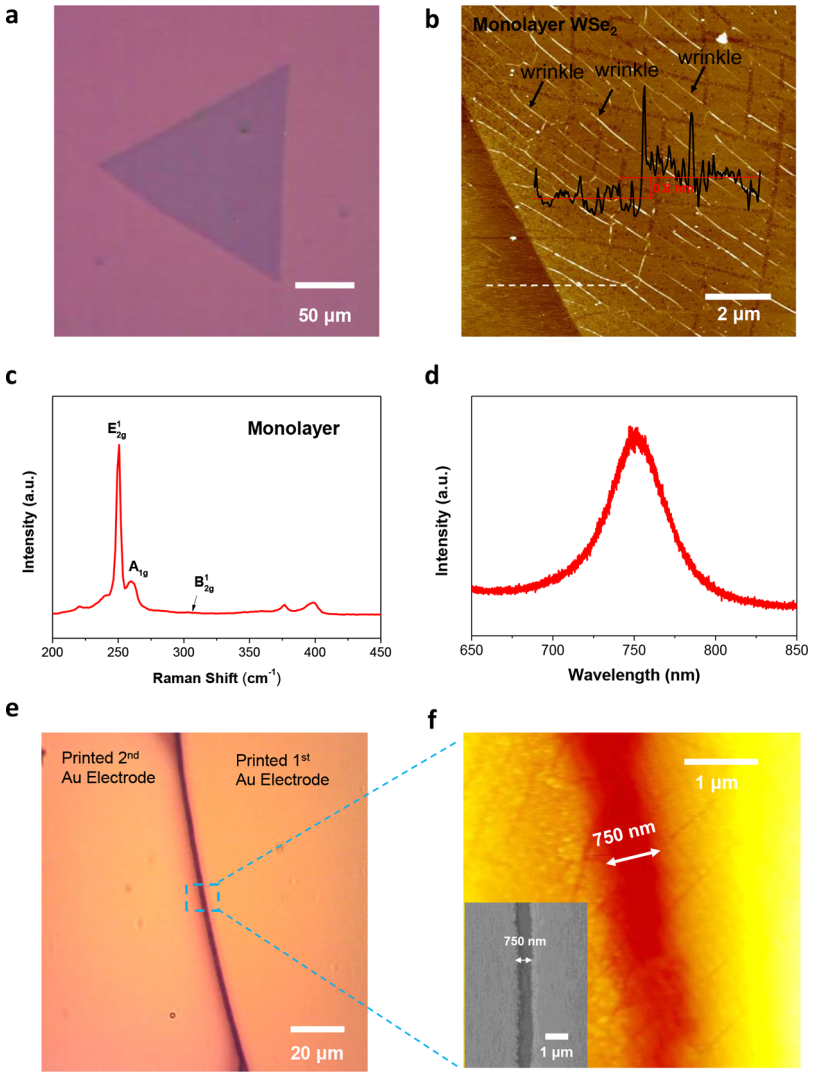

Figure 2. (a–d) Images and characterizations of CVD monolayer WSe_2. (a) Optical microscope image showing a typical triangle-shape monolayer WSe_2 flake transferred to Si/SiO_2. This particular flake is ~187 μm. (b) AFM image of the WSe_2 flake in (a) along with the cross-section height profile of the white dashed line. The thickness of this flake is measured to be ~0.8 nm, corresponding to a monolayer TMDC. (c) Raman spectrum of a typical transferred WSe_2 flake showing the two characteristic peaks of the E^1_{2g} mode and A_{1g} mode. (d) PL spectrum of the same WSe_2 flake in (c) showing a strong PL peak at ~752 nm, confirming the monolayer status. (e) Optical microscope image of a sub-micrometer channel defined by the "flood–dike" printing approach. (f) AFM and SEM (inset) images showing a clearly defined gap measured to be ~750 nm.

materials as the channel materials,[36,48] while we reported a top-contact self-aligned printing method for sub-micrometer FETs with CNTs as the channel materials.[49] The traditional self-aligned printing method works in an "overlap–dewet" fashion, meaning that the second metal electrode is intentionally printed to partially overlap with the self-assembled monolayer (SAM)-coated first electrode and then slowly dewets from the first electrode, yielding a sub-micrometer gap.[36,48,49] However, we have found that this traditional self-aligned printing strategy is not suitable when applied to 2D TMDCs due to the extraordinary wetting properties of the gold ink on the TMDC surface. Specifically, during the printing of the second electrode, the gold ink wets the surface of the TMDC flake so well that it affects the dewetting process of the second electrode, leaving a significant amount of short circuits. Hence, a modified self-aligned printing strategy needs to be developed for 2D TMDC materials.

Here, we report a three-step "flood–dike" self-aligned printing method that can reliably produce sub-micrometer channels on 2D TMDC flakes. In this study, we chose CVD-synthesized monolayer WSe_2 as the channel materials for demonstration. This printing strategy is highly compatible with other CVD-synthesized, mechanically exfoliated, and liquid exfoliated 2D TMDC materials. As the first step, gold nanoparticle ink is printed on the WSe_2 flake to form the first contact electrode. As the second step, a hydrophobic thiol SAM of 1*H*,1*H*,2*H*,2*H*-perfluorodecanethiol (PFDT) is utilized to modify the surface of the gold electrode by lowering the surface tension, making the surface highly hydrophobic.[36,50] The formation of the SAM layer on the gold electrode surface is facilitated by the formation of Au–S covalent bonds between the thiol SAM and gold,[51] while the thiol SAM does not assemble on the pristine WSe_2 surface or the bare Si/SiO_2 surface.[50] As the last step, gold ink is printed close to the first electrode at a certain distance. Due to the good wettability of

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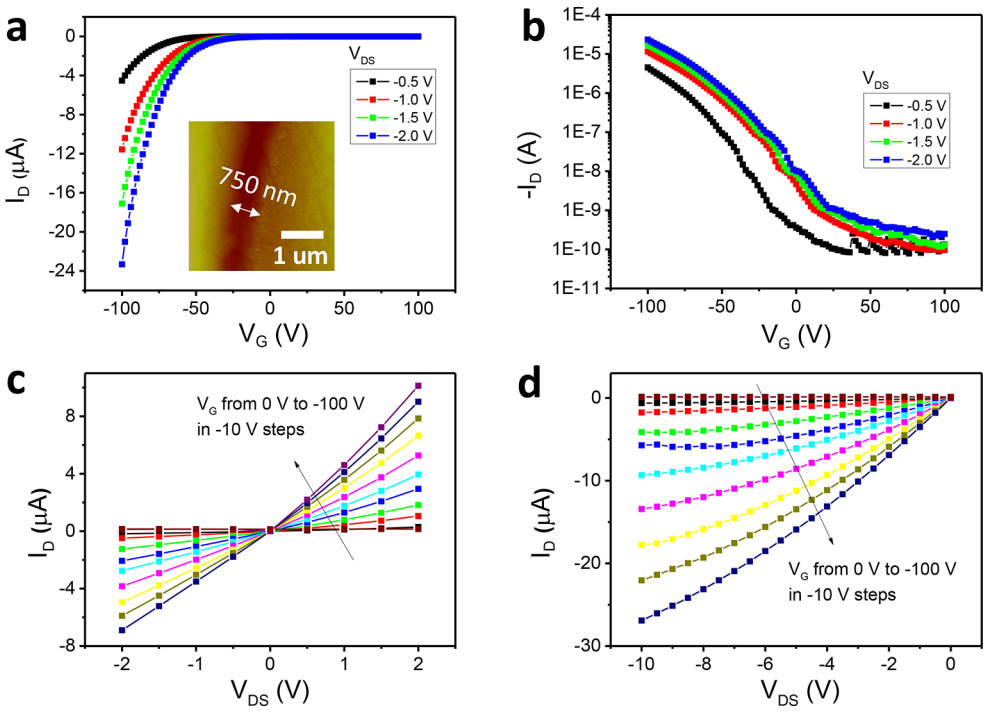

Figure 3. Electrical characteristics of the printed ultrashort channel WSe_2 FET with a back-gate device structure. (a) Transfer characteristics (I_D−V_G) of a typical WSe_2 FET (L = 750 nm, W = 30 μm) measured under different V_{DS} from −0.5 to −2.0 V in steps of −0.5 V. The inset shows the AFM image of the channel, measured to be 750 nm. (b) The same transfer characteristics plotted in a logarithmic scale showing an I_{on}/I_{off} ratio of 1 × 10^5. (c, d) Output characteristics (I_D−V_{DS}) of the same device measured under different V_G from 0 to −100 V in steps of −10 V, with (c) showing the low V_{DS} region and (d) showing the high V_{DS} region, respectively.

the gold ink on the WSe_2 surface, the ink will "flood" toward the first electrode and then be stopped by the hydrophobic SAM coating on the first electrode, ending up drying in close proximity, but not electrically connected, with the first electrode. With this "flood−dike" self-aligned printing method, we have successfully formed gold contacts on WSe_2 flakes with ∼750 nm channel lengths with a ∼90% yield. The as-printed WSe_2 FETs show dramatically improved on-state current densities of ∼0.64 μA/μm (average), high on/off current ratios of ∼3 × 10^5 (average), and good field-effect mobilities of ∼1.0 cm^2/(V s) (average). Compared to previously reported printed 2D TMDC FETs, we have successfully downscaled the channel length to sub-micrometer scale and promoted the on-state current density by several orders of magnitude. Furthermore, with these superior printed WSe_2 transistors, we have successfully demonstrated the driving capabilities for quantum dot (QD) light-emitting diodes (LEDs), inorganic LEDs, and organic LEDs. Overall, our work offers a lithography-free low-cost platform to produce high-performance 2D TMDC electronics and may enable display backplane, sensing, and many other potential applications.

RESULTS AND DISCUSSION

Sub-micrometer WSe_2 FETs were printed on a Si/SiO_2 (285 nm oxide) substrate with a back-gate device structure. To start, high-quality monolayer WSe_2 flakes were synthesized using an ultrafast catalytic growth method on reusable gold foils[52] and then were transferred onto Si/SiO_2 (Figure 1a) by a nondestructive electrochemical bubbling method[52−54] to initiate the three-step "flood−dike" self-aligned printing process. As the first step, gold nanoparticle ink was printed with an inkjet printer on the WSe_2 flake to form a top contact (Figure 1b), followed by sintering in air at 220 °C for 1 h to remove the solvent. We used X-ray photoelectron spectroscopy (XPS) to examine WSe_2 after the annealing step, and the XPS data (Figure S1) indicated slight oxidation of WSe_2, which is qualitatively consistent with our previous observation.[55] As the second step, a thiol-based perfluorinated SAM (PFDT) was used to functionalize the surface of the first electrode to make it repulsive to gold ink (Figure 1c). Lastly, the second electrode was printed close to the edge of the first electrode at a certain distance (Figure 1d,e). After the fresh gold ink contacted the surface of CVD WSe_2, it spread on the flake and flooded toward the edge of the first electrode (Figure 1e), due to the good wetting property between the gold ink and the WSe_2 flake. The SAM coating on the first electrode served as a "flood−dike" and blocked the ink flow of the second electrode from touching the first gold electrode, yielding a sub-micrometer channel in between (Figure 1f). The sample was then sintered in air at 220 °C for 1 h to conclude the printing process.

We used both energy-dispersive X-ray (EDX) and contact angle measurement using a water droplet to confirm the selective formation of the SAM on the surface of the first gold electrode, as described in detail in the Supporting Information (Figures S2 and S3). In addition, we have studied the wetting between the gold ink and WSe_2 surface, SiO_2 surface, fresh gold surface, and SAM-treated gold surface *via* contact angle measurements, and details can be found in the Supporting Information (Figure S4). The good wettability of the gold ink on the WSe_2 surface was verified by contact angle measurement of a sessile gold ink drop on the WSe_2 surface, showing a static contact angle of 4.8° (Figure S4a). Specifically, the gold ink used in our study was a gold nanoparticle solution with a weight concentration of 40% (purchased from UTDots). For the self-aligned printing of the second electrode, we diluted the

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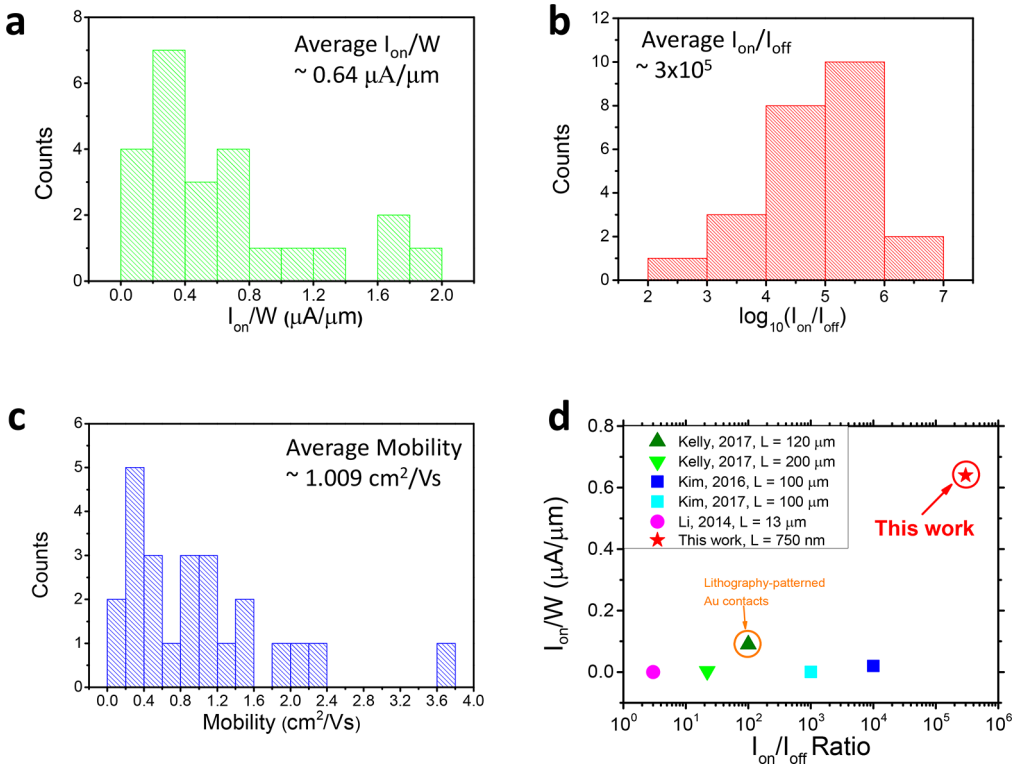

Figure 4. (a–c) Statistical analysis of 24 sub-micrometer WSe_2 FETs printed using the three-step "flood–dike" printing method. (a) Histogram showing the on-state current density (I_{on}/W) distribution measured at V_{DS} = −2 V and V_G = −100 V. (b) Histogram showing the on/off current ratio (I_{on}/I_{off}) distribution, extracted at V_{DS} = −2 V. (c) Histogram showing the field-effect mobility distribution extracted from I_D–V_G curves measured at V_{DS} = −2 V. (d) Comparison study of on-state current density and on/off current ratio between this work and previously reported printed TMDC works.

gold ink with xylene with a volume ratio of 1:2. We believe the good wettability of the gold ink on the WSe_2 surface can be attributed to the nonpolar nature of xylene used to dilute the gold ink and the dispersive nature of the WSe_2 surface,[56] as evidenced by the rather small contact angle of ∼6.6° of a xylene drop on the WSe_2 surface (Figure S5).

High-quality monolayer WSe_2 was synthesized with a recently reported CVD-based ultrafast growth method on gold foils.[52] The ultrafast growth rate (∼26 μm/s) and the reusability of the gold foil allow a cost-effective and energy-saving way to produce large-size WSe_2 within a minute. After growth, a nondestructive electrochemical bubbling method[52−54] was adopted to transfer the as-synthesized monolayer WSe_2 flakes to Si/SiO_2. Figure 2a shows the optical microscope image of a typical transferred triangular WSe_2 flake on Si/SiO_2. This particular flake has a lateral size of 187 μm. Atomic force microscopy (AFM) inspection was performed on this WSe_2 flake as shown in Figure 2b. The cross-section height profile along the white dashed line presents a clear step with a height of ∼0.8 nm, which is close to the thickness of a monolayer WSe_2. The wrinkles on the WSe_2 flakes were formed during the CVD synthesis mainly due to the thermal coefficient mismatch between gold and WSe_2.[52] Raman and photoluminescence (PL) spectra were further conducted to verify the properties of the CVD-grown WSe_2. Figure 2c is a Raman spectrum measured with an incident laser of 561 nm, where both in-plane E^1_{2g} and out-plane A_{1g} characteristic peaks can be clearly observed. Meanwhile, no Raman peak for the B^1_{2g} mode was found, indicating the monolayer status of the CVD-grown WSe_2 samples. In addition, the monolayer feature was further confirmed by PL measurements where a sharp PL emission peak appeared at ∼752 nm, corresponding to the direct band-gap transition of monolayer WSe_2 (Figure 2d).

After the three-step "flood–dike" printing process, the as-formed ultrashort channels were first examined using optical microscopy. Figure 2e shows a representative optical microscope image of an ultrashort channel defined by the "flood–dike" printing method (more images are shown in Figure S6 and Figure S7). From this image, a clean gap can be seen between the two printed gold electrodes. A representative low-magnification optical microscope image can be found in the Supporting Information, Figure S8. AFM was used to further characterize the channel area to get an accurate estimation of the channel length. Based on the AFM characterization of 24 devices, the channel lengths fell in the range of 500–750 nm with little device-to-device variation. Figure 2f shows the AFM image of the channel region of the device shown in Figure 2e, with a measured channel length of ∼750 nm. SEM characterization (inset of Figure 2f) of the same device confirmed the channel length to be ∼750 nm.

The electrical performance study of the printed ultrashort channel back-gated WSe_2 FETs was conducted and is presented in Figure 3. All the transfer and output characteristics of the WSe_2 FETs were carried out in an ambient condition. Figure 3a shows the transfer characteristics (I_D–V_G) of a representative WSe_2 FET, with a channel length (L) of 750 nm (measured by AFM, as shown in the inset of Figure 3a) and a channel width (W) of 30 μm, under different drain voltages (V_{DS}) from −0.5 to −2.0 V in steps of −0.5 V. A clear unipolar p-type behavior was observed from the transfer characteristics, consistent with

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previously reported CVD-WSe_2 FETs with transferred gold contacts.[52] The success in channel length downscaling allows the printed WSe_2 FET to achieve a high on-state current density (I_{on}/W) of 0.78 μA/μm at V_G = −100 V and V_{DS} = −2 V. The same transfer characteristics were also plotted in a logarithmic scale to extract the on/off current ratio (I_{on}/I_{off}) (Figure 3b). Figure 3b clearly shows that the printed ultrashort channel WSe_2 FET has a high I_{on}/I_{off} of ∼1 × 10^5 at V_{DS} = −2 V. The effective mobility (μ_{eff}) under V_{DS} = −2.0 V was extracted with a value of 1.19 $cm^2/(V\ s)$, which is comparable with the previously reported values for CVD monolayer TMDCs;[14,43,46] however this value is lower than the reported values (100−150 $cm^2/(V\ s)$) for the same kind of WSe_2 with transferred electrodes.[52] The reason could be the transferred electrode method minimizes the damage on WSe_2 during the device fabrication process, while our printed devices may have more defects because of the multiple-step treatment process. In addition, the molecular residue from surfactants used in the gold ink may contaminate the Au/WSe_2 interface, which will decrease the mobility as well. We believe this mobility still has significant room for further improvement by optimizing the device fabrication parameters and finding better ways to engineer or treat the gold ink. Study of the hysteresis of the transfer characteristics of the printed WSe_2 FET can be found in the Supporting Information (Figure S9). Output characteristics (I_D−V_{DS}) under small V_{DS} bias (Figure 3c) are very linear, suggesting ohmic contacts between the gold electrode and WSe_2. When a large V_{DS} bias was applied, a clear current saturation can be observed due to the pinch-off effect (Figure 3d), which is typical for p-type (hole) transport.

In order to assess the reliability and uniformity of the "flood−dike" printing method, 24 back-gated FETs have been printed on Si/SiO_2 based on ultrafast-CVD monolayer WSe_2, and their electrical characteristics have been tested. Key device parameters, such as I_{on}/W, I_{on}/I_{off}, and μ_{eff}, were extracted from the transfer characteristics, and systematic statistics analysis was carried out, as shown in Figure 4. Figure 4a shows the distribution of on-state current density for these 24 devices measured at V_{DS} = −2 V and V_G = −100 V. The on-state current densities fell in the range of 0.07−1.86 μA/μm with an average value of 0.64 μA/μm. The distribution of the on/off current ratio (Figure 4b) shows good uniformity with an average value of 3 × 10^5. Furthermore, the distribution of the field-effect mobilities of these devices is presented in Figure 4c, with an average mobility of 1.0 $cm^2/(V\ s)$ and the highest mobility reaching 3.6 $cm^2/(V\ s)$, which is much higher than the values for TMDC nanosheet networks[44,45] and comparable to the previous reported CVD TMDC with printed contacts.[43] Regarding the device-to-device variations in the on-state current density and mobility, we believe an important factor can be the material quality variation from location to location and from flake to flake. This degree of device-to-device variation is actually comparable to the variations observed in other WSe_2 FETs with fabricated metal contacts.[55,57] Besides this factor, we believe other factors, such as wrinkles on the WSe_2 flakes, contact resistance variation, and channel length variation may also contribute to the device-to-device variations.

To fully reveal the advantages of using the "flood−dike" printing strategy for printed TMDC electronics, a comparison of the on-state current density and on/off current ratio was carried out (as shown in Figure 4d), between this work and previously reported printed TMDC works.[43−46] Benefiting from the successful downscaling of the transistor channel length, our printed monolayer WSe_2 possesses a significantly enhanced on-state current density of 0.64 μA/μm (average), which is much higher than previously reported values (Figure 4d). At the same time, the printed sub-micrometer WSe_2 FETs have the highest on/off current ratio of 3 × 10^5 (average).[43−46] We note that previously reported printed 2D TMDC works and this work have used different TMDC species (*e.g.*, MoS_2, WSe_2), different material preparation methods (*e.g.*, liquid exfoliation and CVD), different dielectric materials (*e.g.*, SiO_2, poly(4-vinylphenol), ionic liquid, and boron nitride/ionic liquid), different contacts (*e.g.*, printed Au, printed Ag, printed poly(3,4-ethylenedioxythiophene)polystyrenesulfonate, printed graphene nanosheet network, and fabricated Au), different device structures (*e.g.*, top-gate, back-gate), and different measurement conditions (*e.g.*, different V_{DS}, V_G). The data points presented in Figure 4d were extracted from the electrical characteristics measured at comparable gate voltages and drain voltages. Specifically, the magenta-color data point represents an I_{on}/W of 6 × 10^{-7} μA/μm and an I_{on}/I_{off} of 3 at V_G = −30 V and V_{DS} = 1 V for back-gated FETs with printed MoS_2 ink as channel, printed Ag contacts, and 300 nm SiO_2 as dielectric.[44] The light green data point shows an I_{on}/W of 0.003 μA/μm and an I_{on}/I_{off} of 22 at V_G = −2.5 V and V_{DS} = 1 V for printed WSe_2 nanosheet network FETs with printed graphene network electrodes and boron nitride/ionic liquid hybrid dielectric.[45] The dark green data point represents an I_{on}/W of 0.09 μA/μm and an I_{on}/I_{off} of 100 for printed WSe_2 nanosheet network FETs with lithography-patterned Au contacts and ionic liquid as the dielectric.[45] The on-state current density of these solution-processed TMDC network devices is mainly limited by massive flake-to-flake junctions existing in a long channel with a channel length on a scale of 13−200 μm. Moreover, the dark blue data point shows an I_{on}/W of 0.02 μA/μm and an I_{on}/I_{off} of over 10^4 measured at V_{DS} = 2 V and V_G = 20 V for CVD monolayer MoS_2 FETs with printed Ag contacts and a 270 nm SiO_2 gate dielectric.[43] Last but not least, the light blue data point represents an I_{on}/W of 0.0005 μA/μm and an I_{on}/I_{off} of 10^3 measured at V_{DS} = 1 V and V_G = 80 V for CVD monolayer MoS_2 FETs with printed poly(3,4-ethylenedioxythiophene)-polystyrenesulfonate (PEDOT:PSS) contacts and a poly(4-vinylphenol) (PVP) gate dielectric.[46] With CVD-synthesized continuous MoS_2 film, a significant amount of grain boundaries can exist within a channel of 100 μm, which would consequently compromise the on-state current density.[43,46] A detailed comparison between this work and other reported works can be found in the Supporting Information, Table S1. To sum up, the CVD monolayer WSe_2 sub-micrometer FETs fabricated using the "flood−dike" printing method show clear advantages in terms of high current-driving capacity and good on/off ratio, offering a great platform for making high-performance TMDC macroelectronics aiming for potential display backplane and sensing applications.

On the basis of the enhanced current-driving capacity, high on/off current ratio, and decent mobility of the printed ultrashort channel monolayer WSe_2 FETs, we further explored their applications in display backplane electronics. As a proof of concept, we connected a typical printed WSe_2 FET (L = 750 nm, W = 142 μm) to an external quantum dot-based double heterojunction nanorod LED (QDLED), inorganic LED, and organic LED (OLED), respectively, to demonstrate the LED modulation capability of our printed WSe_2 device. The transfer characteristics of this particular WSe_2 FET can be found in the Supporting Information, Figure S10. The schematic diagrams of

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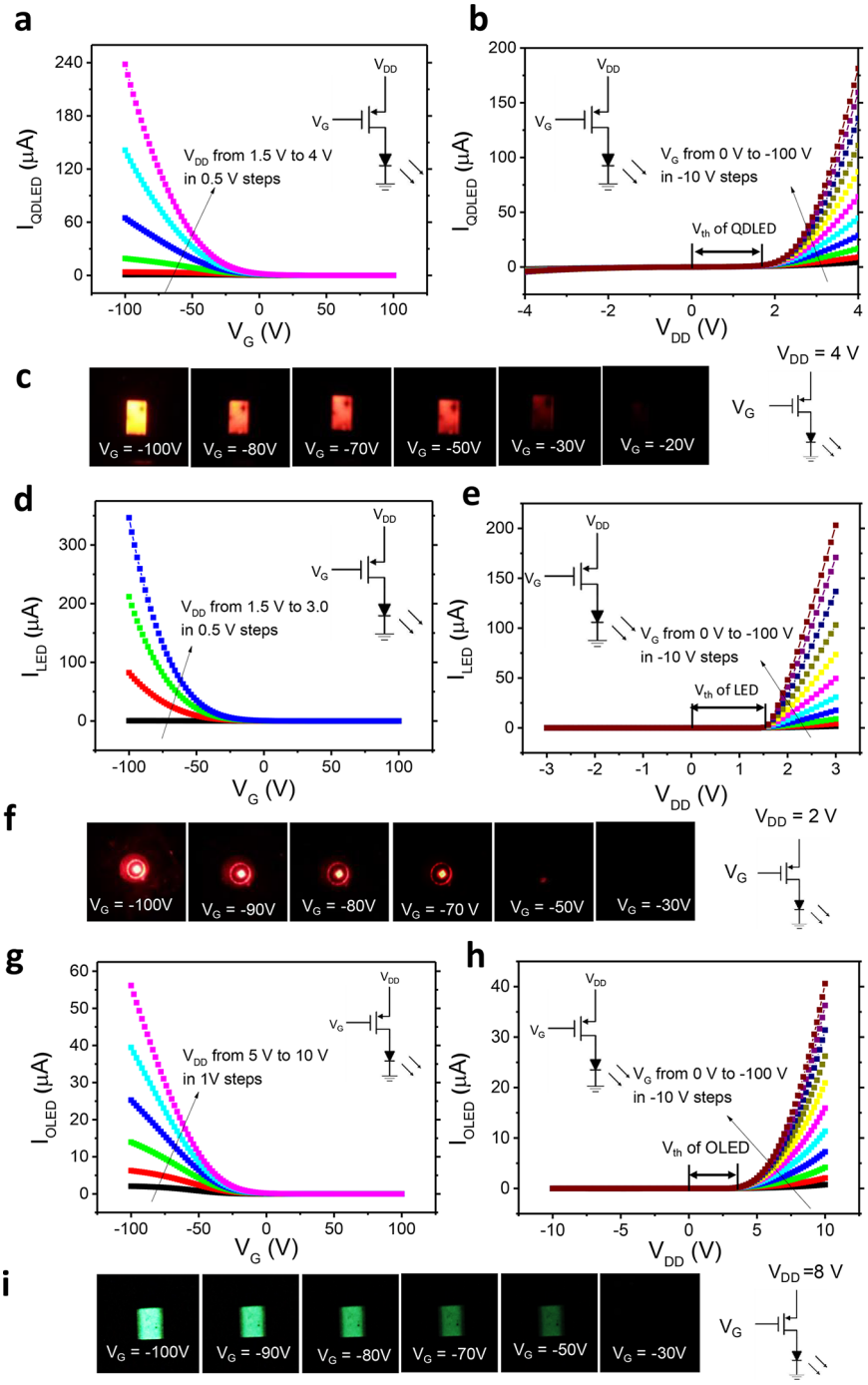

Figure 5. Printed back-gated sub-micrometer WSe_2 FET for QDLED, inorganic LED, and OLED control. (a, b) Electrical characteristics of the printed WSe_2 FET connected to an external QDLED with the circuit diagram shown in the inset. (a) I_{QDLED}−V_G family of curves measured under different V_{DD} from 1.5 to 4.0 V in steps of 0.5 V. (b) I_{QDLED}−V_{DD} family of curves measured under a V_G from 0 to −100 V in steps of −10 V. (c) Optical images demonstrating the light intensity modulation of QDLED by tuning V_G at V_{DD} = 4 V. (d, e) Electrical characteristics of the printed WSe_2 FET connected to an external inorganic LED with the circuit diagram shown in the inset. (d) I_{LED}−V_G family of curves measured under a V_{DD} from 1.5 to 3.0 V in steps of 0.5 V. (e) I_{LED}−V_{DD} family of curves measured under a V_G from 0 to −100 V in steps of −10 V. (f) Optical images showing the light intensity modulation of an inorganic LED by tuning V_G at V_{DD} = 2 V. (g, h) Electrical characteristics of the printed WSe_2 FET connected to an external OLED with the circuit diagram shown in the inset. (g) I_{OLED}−V_G family of curves measured under a V_{DD} from 5 to 10 V in steps of 1 V. (h) I_{OLED}−V_{DD} family of curves measured under a V_G from 0 to −100 V in steps of −10 V. (i) Optical images showing the light intensity modulation of the OLED by tuning the V_G at V_{DD} = 8 V.

the testing circuit are shown in the insets of Figure 5. First, when the printed FET was connected to an external QDLED (the energy band diagram and structure shown in Figure S11a,b), the current flowing through the QDLED (I_{QDLED}) was measured as a function of V_G at V_{DD} from 1.5 to 4 V in 0.5 V steps (Figure 5a). As V_{DD} = 4 V, I_{QDLED} was as high as 240 μA at V_G = −100 V and as low as 3 nA at V_G = 100 V, corresponding to a modulation of I_{QDLED} of 8×10^4. A family of I_{QDLED}−V_{DD} curves at different V_G from 0 to −100 V in −10 V steps (Figure 5b) showed a good diode behavior with a clean

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cutoff region and triode region at different V_G, which suggests a good control over the QDLED. From Figure 5b, the cutoff voltage of V_{DD} is ~1.7 V, in accordance with the turn-on voltage of the QDLED (I–V characteristics of the QDLED shown in Figure S11c).[58] Figure 5c shows a series of photographs of the QDLED taken under different V_G when V_{DD} was fixed at 4 V, illustrating the light intensity modulation. The QDLED was the brightest when V_G = −100 V (first image in Figure 5c) and got gradually dimmer with increasing V_G (second to fifth image in Figure 5c). Eventually, the QDLED was completely turned off when V_G = −20 V (sixth image in Figure 5c).

Similarly, a commercial inorganic LED was externally connected to this printed FET to demonstrate the switching capability for traditional inorganic LEDs. The current–voltage characteristics of the inorganic LED can be found in the Supporting Information, Figure S12. A family of I_{LED}–V_G curves under different V_{DD}'s from 1.5 to 3.0 V in 0.5 V steps are shown in Figure 5d. A closer inspection of Figure 5d indicates that at V_{DD} = 2 V the LED current is ~83 μA when V_G = −100 V, which offered enough brightness for the LED (first image in Figure 5f), and the current fell below 1 nA when the $V_G \geq$ 60 V, corresponding to a modulation of the I_{LED} of 8.3×10^4. Figure 5e shows the I_{LED}–V_{DD} family of curves under V_G from 0 to −100 V in −10 V steps, from which a typical diode behavior can be observed with a cutoff V_{DD} of ~1.5 V, suggesting a good switching capability over the inorganic LED. Images of the LED shown in Figure 5f show that the LED emission light faded with increased V_G and was fully turned off at $V_G \approx$ −30 V. Moreover, current-driving functionality of the printed WSe_2 FET over the OLED (structure and electrical characteristics shown in the Supporting Information, Figure S13) was also demonstrated (Figure 5g–i). Based on the I_{OLED}–V_G family of curves shown in Figure 5g, when the V_{DD} = 8 V and V_G = −100 V, I_{OLED} reached 25 μA, supplying enough current to the OLED, which needs ~1 μA to emit observable light.[29,32] The I_{OLED} is ~1 nA when V_G = 60 V. This corresponds to a modulation of I_{OLED} of 2.5×10^4. A good diode behavior can also be observed from the I_{OLED}–V_{DD} family of curves under different V_G (Figure 5h), showing a cutoff voltage of V_{DD} = 3.5 V, which matches the threshold voltage of the OLED (Figure S13b).[29] Figure 5i shows the OLED light modulation by tuning V_G at a fixed V_{DD} of 8 V, corresponding to the dark blue curve in Figure 5g. When V_G was −100 V, the OLED was very bright (first image in Figure 5i). The light intensity decreased with V_G increasing (second to fifth image in Figure 5i). The OLED was eventually turned off at V_G = −30 V (sixth image in Figure 5i). Overall, we have successfully demonstrated the good control capability of the printed ultrashort channel WSe_2 FET over three different LEDs, including a QDLED, inorganic LED, and organic LED, which lays a good foundation for using printed TMDC electronics for more complicated display control circuits and other potential applications.

It is worth mentioning that the "flood–dike" printing strategy is not limited to the specific type of CVD WSe_2 used in this work. Indeed, it can serve as a general printing strategy to produce high-performance ultrashort channel TMDC devices. This printing method is highly compatible with various CVD-grown TMDC flakes, liquid-exfoliated TMDC inks, continuous TMDC film, *etc.* By scaling down the channel length to sub-micrometer scale, the on-state current density can be enhanced significantly by minimizing the number of flake-to-flake junctions or grain boundaries within the channel. We have also applied this printing approach to monolayer WSe_2 flakes directly synthesized on Si/SiO_2 substrates using a "traditional" CVD method[14,59,60] (as compared to the ultrafast CVD method[52]) and achieved sub-micrometer WSe_2 FETs with a high on-state current of ~0.27 μA/μm (average), a good I_{on}/I_{off} ratio of $\sim 1.6 \times 10^5$ (average), and a high field-effect mobility of ~1.53 $cm^2/(V\ s)$ (average). Details can be found in the Supporting Information, Figures S14–S17. This printing approach also worked well for CVD-synthesized few-layer WSe_2, with a high on-state current density of ~3.6 μA/μm, a decent I_{on}/I_{off} of 10^3, and a high mobility of 10.4 $cm^2/(V\ s)$ (electrical characteristics shown in the Supporting Information, Figure S18). Besides TMDC materials, we believe this printing strategy has the potential to be used for creating sub-micrometer channels on 2D and layered transition metal oxides (TMOs),[61] such as 2D MoO_3, Ga_2O_3, In_2O_3, and ZnO, aiming for high-performance printed devices. Moreover, it is worth mentioning that this printing strategy is not limited to the specific gold ink used in our study. We believe any metal nanoparticle ink that can wet the TMDC surface should be able to work with this method. For example, the silver ink used in ref 43, which was reported to wet MoS_2 well, should be able to work. Furthermore, the substrate of the "flood–dike" printing approach is not limited to Si/SiO_2; it can be easily adapted on flexible or transparent substrates by using a top-gate device structure or electrolyte gate, aiming for wearable and display electronics.

CONCLUSION

In summary, we have successfully demonstrated a "flood–dike" self-aligned printing strategy that offers a lithography-free way to form metal contacts on 2D TMDC materials with sub-micrometer channel length resolution. The use of thiol SAM allows the modification of the surface tension of the first gold electrode to make it more repulsive to the following gold ink, while the surface properties of WSe_2 and SiO_2 remain untouched by the SAM. The contrast in the wetting angles of the gold ink on the SAM-treated Au and the WSe_2 surface enables the gold ink to spread on the WSe_2 surface but be stopped by the SAM coating, thus creating a sub-micrometer channel in a self-aligned manner. By adopting this printing technique, we managed to downscale the transistor channel length of the printed WSe_2 FET to sub-micrometer scale and achieve an enhanced on-state current density of 0.64 μA/μm while maintaining a high on/off current ratio of 3×10^5. The superior performance of the printed WSe_2 FETs allows good controllability over a QDLED, inorganic LED, and OLED. This ultrashort channel printing technique may enable future development of low-cost and high-performance electronics based on 2D TMDCs.

METHODS

Ultrafast CVD Growth and Transfer of High-Quality Monolayer WSe_2 on Au Foils. We grew high-quality monolayer WSe_2 on Au foils by ambient-pressure CVD, as reported previously.[52] A piece of polycrystalline Au foil (99.95 wt %, Alfa Aesar) was well treated with fine polishing and annealing at 1040 °C for over 10 h to reduce its surface roughness before the first use. Then, it was placed in a small quartz boat together with 100 mg of WO_3 powder (99.998 wt %, Alfa Aesar) upstream and loaded at the central zone of a horizontal CVD furnace equipped with a 1-in.-diameter quartz tube. Another small quartz boat that contains 1000 mg of Se pellets (99.99 wt %, Sigma-Aldrich) was placed upstream at the low-temperature zone of

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the furnace. The Au substrate was first heated to 800−950 °C in an Ar atmosphere (100 sccm) and then annealed for 2 min to remove the organics absorbed on its surface. Then we introduced a small flow rate of H_2 (0.5 sccm) to initiate WSe_2 growth. After 1 min, we rapidly stopped the growth by quickly moving the two boats to the low-temperature zone. For structural characterization and device fabrication, the electrochemical bubbling method[52−54] was used to transfer monolayer WSe_2 from Au foils onto Si substrates with a 285 nm SiO_2 dielectric.

Materials Characterization. Raman and PL measurements were performed with a 561 nm laser (Renishaw Raman system). AFM (Digital Instrument, DI 3100) was conducted to inspect the thickness of the as-grown WSe_2 samples. AFM and SEM (Hitachi S4800 with an electron accelerating voltage of 1 kV) were used to inspect the channel length of the printed WSe_2 FETs.

Three-Step "Flood−Dike" Printing Method. The first Au electrodes were printed onto the CVD WSe_2 flakes using an inkjet printer (Microplotter Desktop, SonoPlot, Inc.) followed by sintering at 220 °C for 1 h to remove the solvent in the Au inks (UTDAu40IJ, UT Dots, Inc.). Then, the sample was immersed in a solution consisting of PFDT (97%, Sigma-Aldrich) and isopropyl alcohol (IPA) in a volume ratio of 1:10 for 18 h. During this functionalization step, PFDT molecules will be selectively deposited on the surface of the first printed electrodes, forming a self-assembled monolayer. This selective deposition of PFDT on the Au surface was facilitated by forming Au−S covalent bonds between Au and thiol.[51] After functionalization, the sample was gently rinsed with IPA and blown dry with N_2 gas. In the last step, a xylene-diluted gold ink (gold ink:xylene = 1:2) was used to print the second electrodes close to the previous electrodes. A clear screening effect of the ink flow can be observed. The sample was sintered at 220 °C for another 1 h to remove the solvent in the second electrodes.

Fabrication of QDLEDs. Prepatterned indium tin oxide (ITO) substrates (15−25 Ω/□, Delta Technologies) were cleaned thoroughly by acetone, methanol, and IPA several times and then treated with UV-ozone for 15 min. Poly(3,4-ethylenedioxythiophene)-polystyrenesulfonate (Clevios P VS AI 4083) was spin-cast on an ITO/glass substrate at 4000 rpm for 30 s and dried in air at 120 °C for 5 min. The substrates were then moved into a glovebox and annealed at 210 °C for 10 min. Then, 2 mg mL^{-1} of 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F_4TCNQ, Sigma-Aldrich) and 5 mg mL^{-1} of poly[(9,9-dioctylfluorenyl-2,7-diyl)-*co*-(4,4′-(*N*-(4-*s*-butylphenyl))-diphenylamine)] (TFB, H. W. Sands Corp.) in *m*-xylene were spin-cast at 3000 rpm for 30 s and baked at 180 °C for 30 min. Double-heterojunction nanorods (DHNRs)[58] were purified using a mixture of chloroform and methanol. DHNRs were dispersed in chloroform and spin-cast (2000 rpm for 30 s) on top of the TFB/F_4TCNQ layer, then subsequently annealed at 180 °C in the glovebox (30 min). ZnO was synthesized using the same method as described previously.[58] In brief, a solution of potassium hydroxide (1.48 g) in methanol (65 mL) was added to a zinc acetate dihydrate (2.95 g) solution in methanol (125 mL), and the reaction mixture was stirred at 60 °C for 2 h. The mixture was then cooled to room temperature, and the precipitate was washed twice with methanol. The precipitated ZnO (~30 mg mL^{-1} in butanol) was spin-cast at 3000 rpm for 30 s and annealed at 110 °C for 30 min. Samples were then taken out of the glovebox and loaded into an electron-beam evaporator, where a 100 nm thick Al cathode was deposited at a rate of 0.1−0.2 nm/s. LED devices were brought back into the glovebox and encapsulated by epoxy (Norland Optical Adhesive 86) and a glass coverslip.

Fabrication of OLEDs. Organic light-emitting diodes were fabricated on prepattered ITO anodes on glass. The substrates were cleaned by a gentle detergent scrub followed by successive sonications of 15 min each in water, acetone, and IPA and a 10 min UV-ozone treatment. The device structure for the OLEDs was ITO/NPD (50 nm)/Alq_3 (50 nm)/LiF (1 nm)/Al (100 nm). NPD (*N*,*N*′-diphenyl-*N*,*N*′-bis(1-naphthyl)-1,1′-biphenyl-4,4″-diamine) and Alq_3 (tris(8-hydroxyquinoline)aluminum) were supplied by Universal Display Corporation and were used as received. The organic layers and cathode were deposited by vacuum thermal evaporation (Angstrom Engineering) with a base pressure of less than 10^{-6} Torr. Organic layers were deposited at evaporation rates of 1 Å/s, and LiF was deposited at a rate of 0.2 Å/s. An aluminum cathode was deposited through a metal mask at a rate of 1−2 Å/s in a cross-bar structure defining device areas of 4 mm^2. Devices were encapsulated with epoxy and a cover glass inside the nitrogen glovebox prior to exposure to ambient environment.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.7b06654.

XPS data of WSe_2, study of wetting properties of gold ink on WSe_2, additional images of devices, detailed comparison of device performance between this work and other printed TMDC works, schematics of LED structures, device characteristics of LEDs, and device performance of printed FETs based on WSe_2 flakes directly synthesized on Si/SiO_2 (PDF)

AUTHOR INFORMATION

Corresponding Author

*E-mail: chongwuz@usc.edu.

ORCID

Yihang Liu: 0000-0002-2491-9439
Moonsub Shim: 0000-0001-7781-1029
Mark E. Thompson: 0000-0002-7764-4096
Wencai Ren: 0000-0003-4997-8870
Chongwu Zhou: 0000-0001-8448-8450

Author Contributions

□F. Wu and L. Chen contributed equally.

Notes

The authors declare no competing financial interest.

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