Protocol: Intan RHD2164 Integration with Parylene Microelectrode Arrays

Description: This document details the protocol for integrating the Intan RHD2164 ASIC with Parylene microelectrode arrays (MEAs) by way of polymer ultrasonic on bump (PUB) bonding [1], [2].

Table of Contents

1 Device Design

1.1 pMEA

Note: these guidelines assume that fabrication of pMEAs will include annealing
Materials: *None*
Equipment: *None*

1. Bond pads
    a. The bond pad layout on the pMEA should mirror that of the Intan RHD2164 (Figure 1). Refer to the spec sheet for details on the layout.

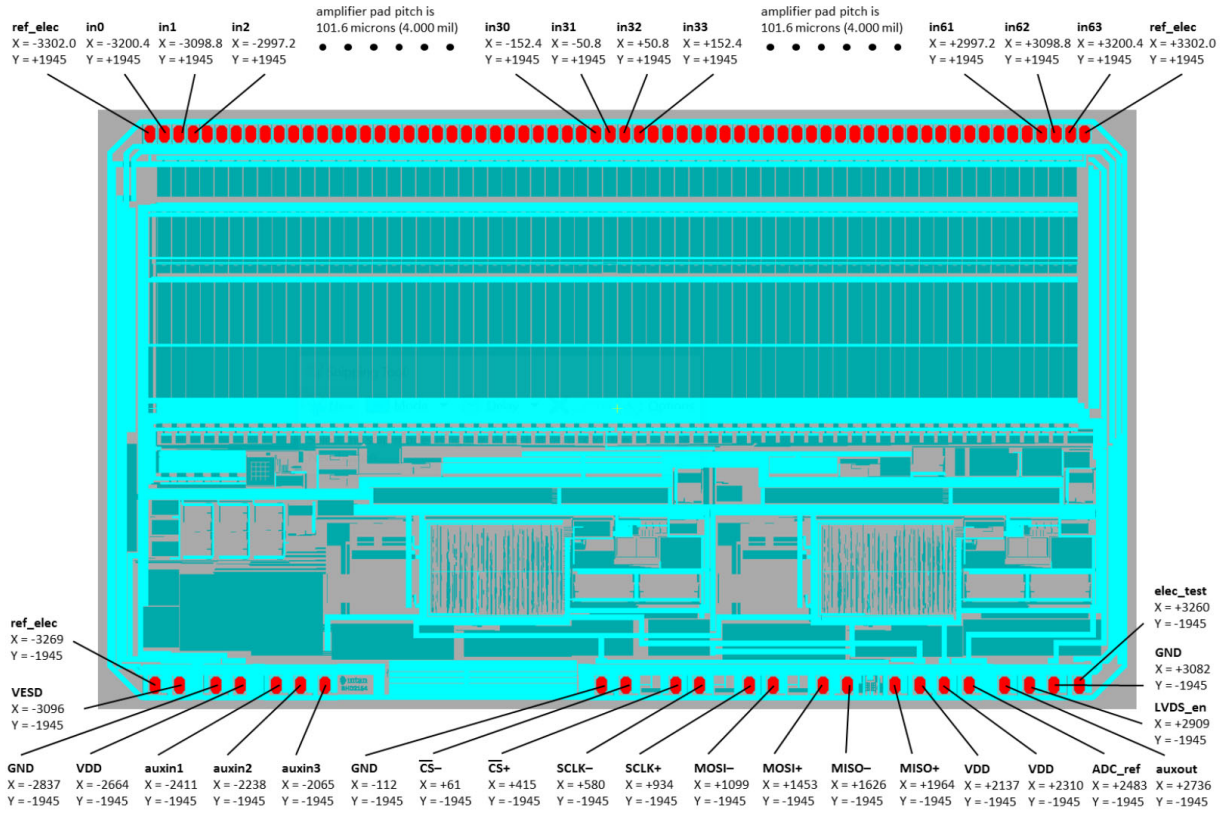


Figure 1: Layout of the Intan RHD2164. Reproduced from [3].

b. Additionally, to account for shrinking of the Parylene during fabrication, bond pad spacing should be increased by 1%.

c. Cutout slots between bond pads are useful for minimizing lateral movement during bonding (Figure 2).

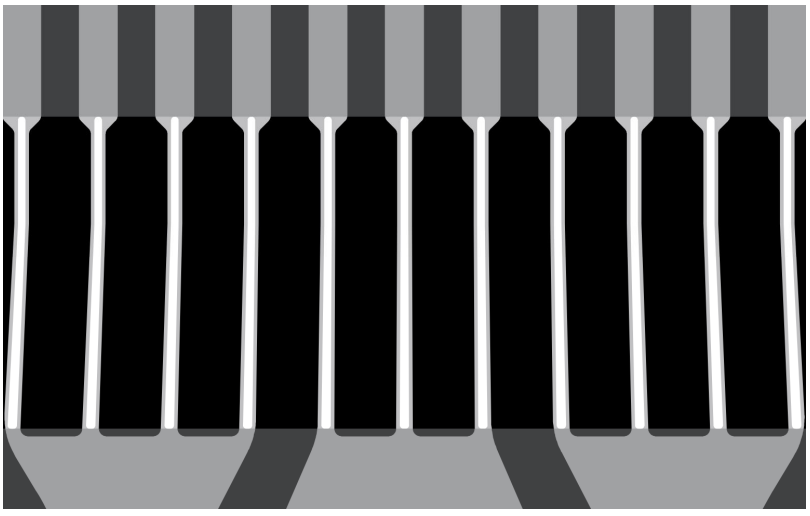


Figure 2: Cutout slots between pads. The width of each slot is 10 µm.

2. Traces
    a. Due to the amount of current that is passed into the ASIC, make all traces from the power lines (VDD, GND) as wide as possible.
        - For reference, up to 16 mA can be used by the chip across 3 pairs of power lines. A 50 µm wide trace with 250 nm of metal on a Parylene substrate can handle a third of this current, but not the full amount.
3. Contact pads
    a. If a zero-insertion force (ZIF) connector is to be used, also increase the contact pad spacing by 1%.
    b. There are 2 pairs of lines that could be tied together on the pMEA (VDD + VDD, GND + VESD), but this may increase the current load on the trace.

1.2 PCB

Materials: *None*
Equipment: *None*

1. As per Intan recommendations for low-voltage differential signaling (LVDS), ensure the following passive components are accounted for:
    a. 100 Ω resistor between each pair of CS+ and CS-, CLK+ and CLK-, and MOSI+ and MOSI-.
    b. 100 nF capacitor between voltage and ground
    c. 10 nF capacitor between ADC_ref and ground
    d. See Figure 3 for a schematic of a PCB where 30 electrodes were connected to the ZIF.

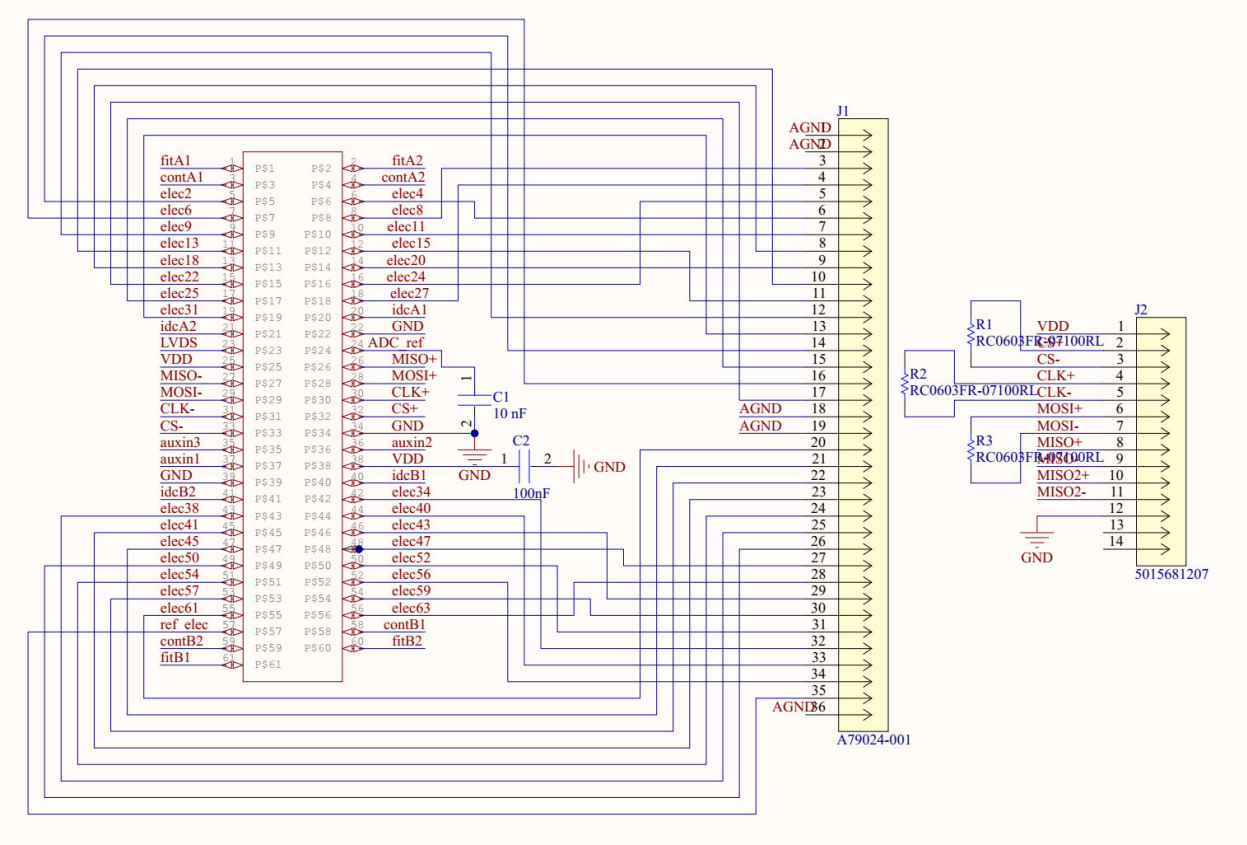


Figure 3: Schematic for an ASIC-integrated pMEA that is routed to an Omnetics and Molex connector

2. Add 2 holes for alignment pins to be press fit later.
    a. Be sure to account for the tolerance of the manufacturer.
    b. When the PCB is received, these holes can be reamed to the proper size.
3. Add a window for aligning the ASIC and pMEA

2 BUMPING

2.1 BALL BONDING

Materials: *Au Wire*
ASIC (bare die)
Equipment: *Ball bonder*
Bump capillary

1. Place ASIC directly on top of workstage vacuum hole. Turn vacuum ON.
2. Set parameters to the following:

	Bond 1
Ultrasonic	90 mW
Time	80 mS
Force	18 g
EFO	15
Temperature	150 °C
Tail	3.0
Pull	0.2

3. Using the fine pitch bump capillary, place ball bonds on each bond pad (Figure 4).
    a. There is enough space for two, but PUB bonding 2 balls requires more force.
    b. Instead, you can bond to one half of the pad so that in the rare case that bonding fails, you can still utilize the other half.

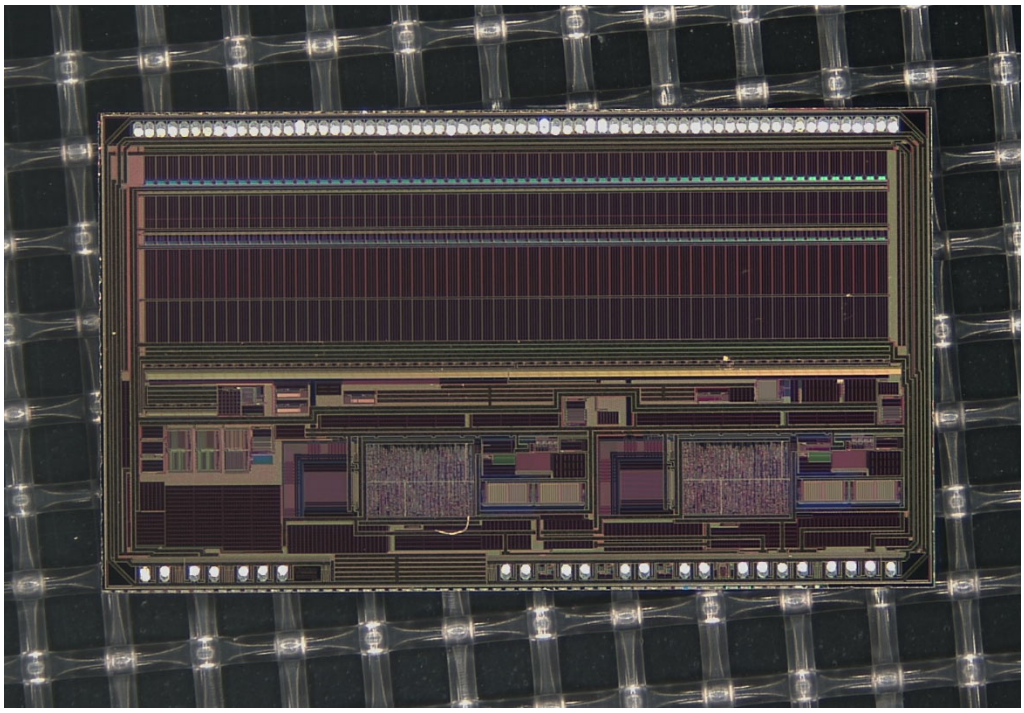


Figure 4: Intan RHD2164 with ball bonds on the pads

4. Once bonding is complete, turn vacuum OFF and remove ASIC from the stage.
5. Repeat on all chips to be bonded.

2.2 BUMPING

Materials: *ASIC with ball bonds*
Equipment: *Wedge Bonder*
Waffle tool

1. Place ASIC directly on top of workstage vacuum hole. Turn vacuum ON.
2. Set parameters to the following:

	Bump	
	Bond 1	Bond 2
Ultrasonic	4.3	4.3
Time	4.4	4.4
Force	0.5	0.5
Temperature	120 °C	
Tail	4.3	
Pull	2.5	

3. Using the bonder, tamp each ball down one at a time.
    a. Hitting 2 balls at a time will require a different force. It is not recommended.
4. Once complete, turn OFF the vacuum and remove ASIC from the stage.
5. Repeat on all chips to be bumped.

3 ALIGNMENT

3.1 DEVICE PLACEMENT

Materials: *Lab tape*
#2-56 screws
#4-40 screws
Alignment PCB
Mylar ZIF backing
Equipment: *Wedge bonder*
Allen wrenches

1. Insert pMEA onto PCB using alignment holes.
2. Connect the ZIF portion of the device to the ZIF connector with the Mylar backing on top of the device (contacts facing down).
3. Fit the device cover over the device and secure with #2-56 (Figure 5).
    a. The depression in the cover is to ensure that the pMEA ribbon cable is not crushed.
    b. The screws will mate from the bottom of the subassembly.

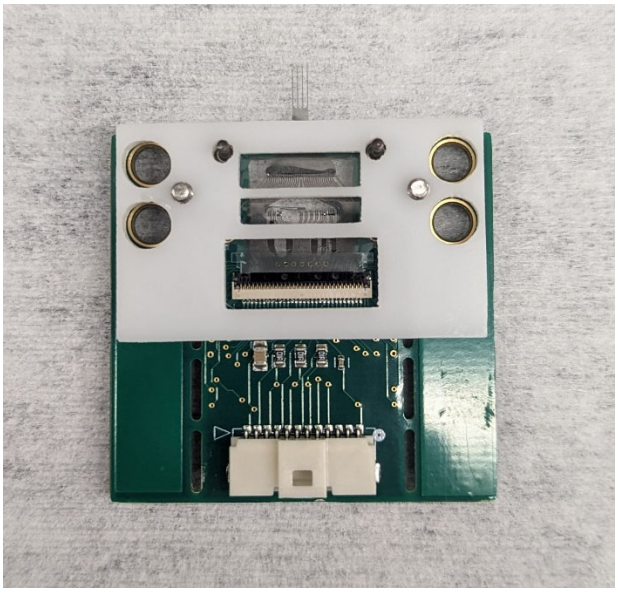


Figure 5: The pMEA should be secured with the device cover.

3.2 ALIGNMENT

1. Place chip holder on wire bonder workstage, aligning the through hole with the vacuum hole Figure 6).

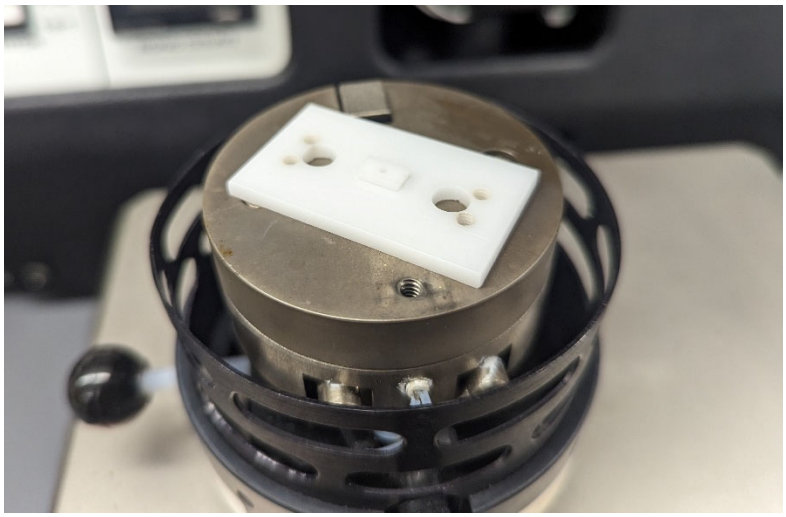


Figure 6: The chip holder should sit on the wire bonder workstage, with the hole lined up with the workstage's vacuum.

2. Secure chip holder to workstage using lab tap along the edge of the holder.
3. Place ASIC onto holder. Then turn on the house vacuum.
4. Connect the 10-pin Molex connector to the PCB.
5. Place 2 #4-40 screws into PCB subassembly then place on top of the chip holder.
6. Using the microscope, move the subassembly until the pMEA and ASIC are aligned.
    a. Initial ASIC placement may be off. If so, turn off vacuum and nudge into place.
    b. Trying to nudge with the vacuum ON can damage the ASIC.
7. Secure with #4-40 screws when alignment is complete.
    a. There are 4 holes, but 2 is sufficient (Figure 7).

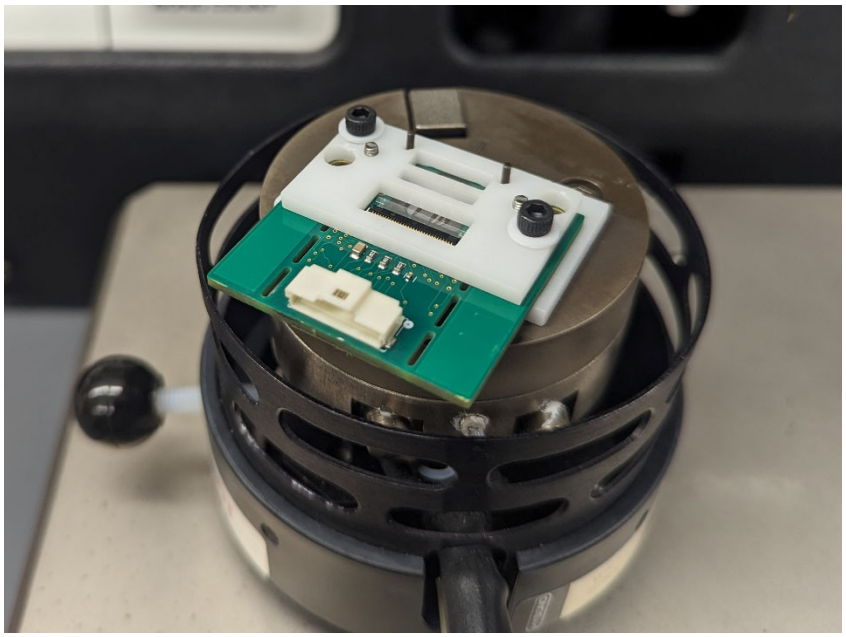


Figure 7: After aligning, the pMEA can be secured to the chip using screws.

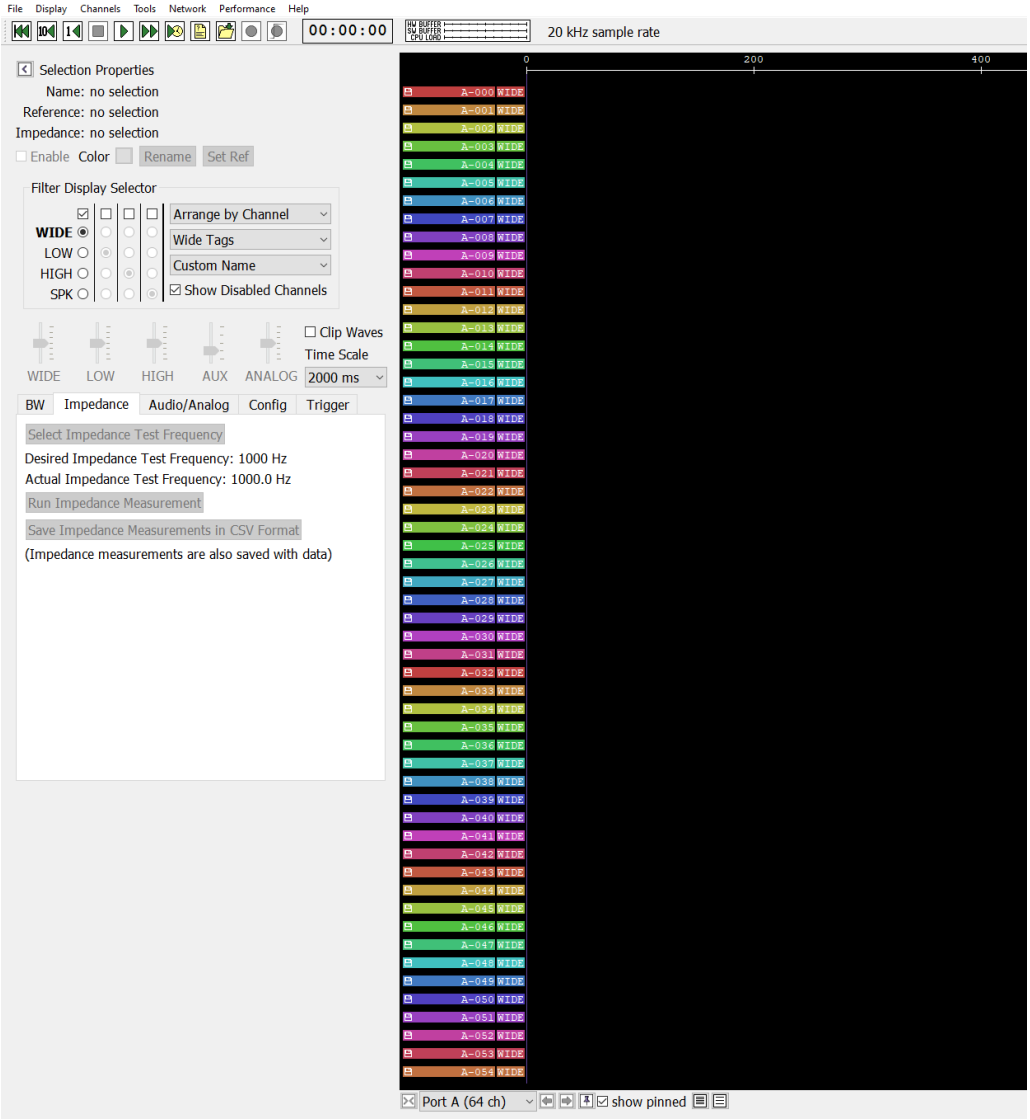
8. Connect Omnetics portion of cable into Intan USB board.

4 PUB BONDING

4.1 BONDING

Equipment: *Wedge bonder*
Tape Automated Bonding (TAB, Waffle) tool

1. Inspect the height difference, if any, between the top of the bumps and the pMEA. If the deflection is greater than the height of a bump (roughly 25 µm), consider reseating the pMEA or shifting the cover to ensure the pMEA and ASIC bumps are as level as possible.
2. Bond select bumps to secure device and chip together.
    a. The device can shift during bonding, but good initial bonding can minimize this.
    b. Start with non-essential bond pads on the digital outputs.
        i. These include auxin1, auxin2, auxin3, auxout, LVDS_en, and elec_test
    c. On the inputs, start in the middle and bond every other or every 3 pads across the entire length.
    d. Go back to the digital outputs and bond all lines.
3. Connect the Intan USB board to the PC and turn on the RHX software.
4. If all digital outputs are connected, you should see 64 channels identified.



   a. If channels are not connected, you can try to rework bonds on the digital lines by using the waffle tool at a slightly higher force.
   b. If the above does not work and if the chip is functional, you can retry the PUB bonding step with a different pMEA.
5. Once functionality is confirmed, disconnect the Omnetics connector from the USB board.
6. Bond all remaining pads.

4.2 UNDERFILL

Note: this step should be performed immediately after Bonding (step 4.1)
Materials: *Epo-Tek 301*
Equipment: *Toothpick*
Fine gauge needle

1. Prepare the epoxy using the scale to weigh.
   a. Ratio of part A to part B by weight is 20:5.
2. Mix thoroughly with a toothpick.

3. Dip the needle tip into the epoxy.
4. Touch one of the slits near the bond pads on the pMEA and let capillary action pull the epoxy between the pMEA and ASIC.
5. Repeat as necessary, avoiding bubbles if possible.
    a. Introducing epoxy from opposite sides runs the risk of creating a bubble when the two "fronts" of epoxy meet.
    b. Best practice may be to place epoxy on one corner and re-apply as necessary.
6. If too much epoxy is applied, use the corner of a Kimwipe to wick it back.
7. Turn the vacuum OFF.
8. Leave the entire setup (chip holder, pMEA subassembly, etc.) on the work stage for 1.5 hours.
    a. Place a droplet of epoxy on a glass slide and place the slide on a hot plate set to 60 °C.
    b. This can act as a proxy for checking curing.
9. Once cured, ASIC-pMEA can be removed from the subassembly.

5 TESTING

5.1 ON-CHIP IMPEDANCE TEST

Materials: *1× PBS*
Equipment: *Beaker*
Lab tape

1. Pour PBS into the beaker.
2. Lower PCB with pMEA into beaker until only the tips are immersed.
    a. Lab tape can be used to secure the PCB
3. Connect 10-pin Molex connector.
4. Connect Omnetics connector to Intan USB board.
5. Connect USB board to PCB.
6. Turn ON RHX software.
7. Open the Properties on the left (may need to click on the arrow)
8. Click on the Impedance tab.
9. Select 1000 Hz if it is not selected already.
10. Run Impedance Measurement.
11. Save measurements in CSV format.
12. You can also run the software (green triangle Play button near the top) or record (red circle) data at this point.

APPENDICES

A. MATERIAL SOURCES

Note: Standard materials (e.g. acetone, DI water, cleanroom wipes, etc.) are not listed

Material	**Supplier**
EPO-TEK MED-301	Epoxy Technology, Billerica, MA
Intan RHD2164	Intan Technologies, Los Angeles, CA
3/64”dowel pins (Catalog #98381A981)	McMaster-CARR, Elmhurst, IL
Au wire	California Fine Wire Company, Grover Beach, CA

B. EQUIPMENT MODELS

Note: Standard equipment (e.g. tweezers, microscopes, N2 gun, scale, etc.) are not listed

Equipment	**Model #**	**Supplier**
Ball bonder	626	Hybond, Escondido, CA
Fine-pitch capillary	SBB-33090-515A-ZP94	Small Precision Tools, Lyss, Switzerland
Wedge bonder	527A	Hybond, Escondido, CA
‘Waffle’ tool	7045W-TI-10050-3/4-M	Small Precision Tools, Lyss, Switzerland
USB interface board	C3100 (discontinued)	Intan Technologies, Los Angeles, CA
Acquisition Board	OEPS-9030 (alternative to above)	Open Ephys, Atlanta, Georgia

C. REFERENCES

[1] J. J. Yoo and E. Meng, “ASIC Integration via Polymer Ultrasonic Bump Bonding to A 64-Channel Penetrating Parylene Multielectrode Array,” in *2024 IEEE 37th International Conference on Micro Electro Mechanical Systems (MEMS)*, Austin, TX, USA: IEEE, Jan. 2024, pp. 392–395. doi: 10.1109/MEMS58180.2024.10439599.

[2] J. J. Yoo and E. Meng, “Bonding Methods for Chip Integration with Parylene Devices,” *J. Micromechanics Microengineering*, Feb. 2021, doi: 10.1088/1361-6439/abe246.

[3] Intan Technologies, LLC, “RHD2164 Digital Electrophysiology Interface Chip.” RHD2164 datasheet, Dec. 01, 2017. Accessed: Nov. 18, 2020. [Online]. Available: https://intantech.com/files/Intan_RHD2164_datasheet.pdf